(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 932 262 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
28.07.1999 Bulletin 1999/30

(51) Int. Cl.[6]: **H04B 1/707**

(21) Application number: **98124528.5**

(22) Date of filing: **22.12.1998**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **26.12.1997 JP 36766397**
05.02.1998 JP 3974698
18.02.1998 JP 5449098

(71) Applicants:
- **Yozan Inc.**
  Tokyo 155-0031 (JP)
- **Ntt Mobile Communications Network Inc.**
  Minato-ku, Tokyo 105-0001 (JP)

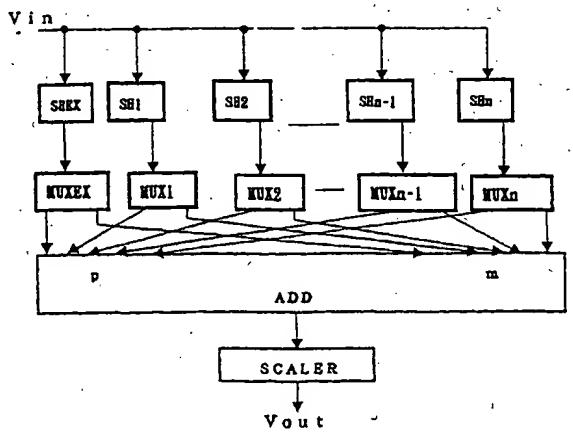
(72) Inventors:
- **Zhou, Changming**
  Tokyo 155-0031 (JP)
- **Zhou, Xuping**
  Tokyo 155-0031 (JP)
- **Sawahashi, Mamura**
  Kanagawa 236-0052 (JP)
- **Adachi, Fumiyuka**
  Kanagawa 236-0052 (JP)

(74) Representative:
Grünecker, Kinkeldey,
Stockmair & Schwanhäusser
Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

(54) Signal reception apparatus for DS-CDMA cellular system

(57) A plurality of sets of spreading code sequences are store in registers and selectively supplied to matched filters. The soft-handover, multi-code processing and long-delay paths can be processed by a small circuits.

Fig.1



EP 0 932 262 A2

Description

Detailed Description of the Invention

Background of the Invention

Field of the Invention

[0001] The present invention relates to a signal reception apparatus for DS-CDMA cellular system having a sampling and holding circuit for holding analog input signal successively, a plurality of matched filters each for calculating a correlation between the input signal and a spreading code and a plurality of calculation registers each corresponding to one of the matched filters for storing the spreading code to be supplied to the corresponding matched filter.

Prior Art

The code division multiple access (CDMA) cellular system above is advantageous for an asynchronous system among base stations it is possible to identify the base stations and mobile stations and it is unnecessary to manage the timing over a plurality of cells. The asynchronous system does not need an external synchronization system, such as a global positioning system (GPS), so its base station can be established by a low cost. In the synchronous system, the base stations are identified by the time difference of signals from base stations reach to a mobile station, rather than by a unique long code, so it likely happens that a base station is incorrectly identified. While, the signal reception apparatus of the mobile station for asynchronous cellular system has a lot of performances, that is, a despread of a composite code of short and long codes, a fading compensation of a multi-path signal, a rake combining, the identification and evaluation of a plurality of base stations for an initial and peripheral cell search, changing of the transmission speed by variable spreading ratio and a multi-code communication for high speed communication. When a mobile station moves over a plurality of cells, base stations should be changed by soft-handover one after another.

[0002] Therefore, the signal reception apparatus for the CDMA cellular system may become complicated and large in circuit size. The signal reception apparatus is not preferable for a mobile station. If a long-delay path is to be processed, a plurality of matched filters are necessary in a traffic channel for one code sequence, so the circuit is further complicated. Also for the multi-code processing and soft-handover processing, a plurality of matched filters are necessary.

Summary of the Invention

[0003] The present invention has an object to provide a signal reception apparatus for DS-CDMA cellular system of small size available for processing by a plurality of spreading codes.

[0004] According to the present invention, one or a plurality of matched filters are connected with a plurality of registers for storing a plurality of spreading codes through a multi-plexer.

Brief Description of the Invention

[0005]

Fig. 1 is a block diagram of a matched filter in a signal reception apparatus for the DS-CDMA cellular system,
Fig. 2 is a block diagram of a register for storing a plurality of spreading codes,
Fig. 3 is a block diagram of a phase-multi-plexer in Fig.2,
Fig. 4 is a timing chart of the matched filter for receiving signals from a plurality of base stations,
Fig. 5 is a block diagram of another matched filter,
Fig. 6 is a circuit diagram of the circuit following to the matched filter,
Fig. 7 is a timing chart of the matched filter for another processing,
Fig. 8 is a timing chart of the matched filter for further another processing,
Fig. 9 is a flow chart of the processing of Fig.8,
Fig. 10 is a timing chart of the matched filter for multi-code processing,
Fig. 11 is a flow chart of the processing of Fig. 10,
Fig. 12 is a flow chart of schedule determination in Fig. 11,
Fig. 13 is a flow chart of receiving in Fig. 10,
Fig. 14 is a timing chart of the matched filter for another multi-code processing,
Fig.15 is a timing chart of the matched filter for long-delay processing when a log-delay does not occur,

Fig. 16 is a block diagram of a register for storing a spreading code for long-delay,

Fig. 17 is a timing chart of the matched filter for long-delay processing when a log-delay occurs,

Fig. 18 is a block diagram of another register for storing a spreading code for long-delay,

Fig. 19 is a block diagram of further another register for storing a spreading code for long-delay,

Fig.20 is a circuit diagram of a multi-plexer in Fig. 1,

Fig. 21 is a circuit diagram of another multi-plexer in Fig. 1,

Fig.22 is a circuit diagram of a sampling and holding circuit in Fig. 1,

Fig.23 is a circuit diagram of a switch in Fig. 1, and

Fig.24 is a circuit diagram of an adder in Fig. 1.

Preferred Embodiment

[0006] Hereinafter, preferred embodiments of a signal reception apparatus for DS-CDMA cellular system according to the present invention are described with reference to the attached drawings.

[0007] In Fig. 1, one of matched filters in a signal reception apparatus includes a plurality of sampling and holding circuits SH1 to SHn parallelly connected to an analog input signal Vin. The sampling and holding circuits are controlled by a system clock so as to successively hold the signal Vin in response to the system clock. Since the signal held by one sampling and holding circuit is not transferred to another sampling and holding circuit, the transfer distortion is avoidable.

[0008] Outputs of the sampling and holding circuits are input to corresponding multi-plexers MUX1 to MUXn of one input and two outputs. Each multi-plexer alternatively outputs the input to one of two outputs in response to a spreading code of one bit. The output of each multi-plexer is input to a plus terminal "p" and a minus terminal "m" of an adder ADD. The terminals "p" and "m" are selected in response to "1" and "0" of the spreading code, and the adder has circuits for adding operation and subtracting operation. An output of the adder ADD is input to a scaling circuit SCALER for scaling the output of the adder to be an adequate level.
An output Vout is generated after the scaling.

[0009] The sampling and holding circuits SH1 to SHn hold the input signal successively and circulatively, that is, SH1, SH2, ..., SHn, then from SH1 to SHn, repeatedly. A spreading code including the spreading codes for the muti-plexers MUX1 to MUXn is circulated so that the relationship between the order of the input signals from the oldest to the newest and the spreading codes is not changed. The multi-plexers MUX1 to MUXn are quickly switched in response to the circulated spreading codes.

[0010] There are provided a plurality of matched filters MF01, MF02, MF11, MF12, MF21, MF22, MF23 and MF24 as shown in Fig.6. Other circuits connected to the matched filters are shown in Fig.6. The number of the matched filters is eight in Fig.6, however, the number can be changed. Among eight matched filters, MF01 and MF02 are allocated to a perch channel group Pch, MF21 to MF24 are to a traffic channel group Tch, and MF11 and MF12 are to a common group Cch.

[0011] The four matched filters of the groups Pch and Cch are connected to a four-inputs-one-output multi-plexers MUXp1 to MUXpS each of which selectively output one of the outputs of the four matched filters. The multi-plexers MUXp1 to MUXpS are connected to multipath-signal sampling and holding circuits SHp1 to SHpS, respectively. Each sampling and holding circuit holds one of peaks in the channel Pch and Cch.

[0012] The matched filters of the groups Tch and Cch are connected to six-inputs-one-output multi-plexers MUXt1 to MUXtR each of which selectively output one of the outputs of the six matched filters. The multiplexers MUXt1 to MUXtR are connected to multi-path-signal sampling and holding circuits SHt1 to SHtR, respectively. Each sampling and holding circuit holds one of peaks in the channel Tch and Cch.

[0013] Outputs of the matched filters of the groups Pch, Tch and Cch are input to a peak detection circuits PDp and PDt. The peak detection circuit PDp detects correlation peaks of the perch channel and/or common channel connected to the circuit PDp and averages each of the peaks for a plurality of periods, then registers phase of higher peaks after sorting of power of the peaks. The peak detection circuit PDt detects correlation peaks of the traffic channel and/or common channel connected to the circuit PDt and averages each of the peaks for a plurality of periods, then registers phase of higher peaks after sorting of power of the peaks. The circuits PDp and PDt output control signals for the sampling and holding circuits SHp1 to SHpS and SHt1 to SHtR. The control signals from PDp and PDt are decoded by decoders DECp and DECt, respectively, into sampling signals for the sampling and holding circuits SHp1 to SHpS and SHt1 to SHtR, respectively. The peak detection is performed corresponding to total or part of the matched filters.

[0014] The matched filters of common group Cch can be used for the perch channel or traffic channel, then the number of matched filters for the traffic channel is available from four to six. The number of matched filters for the perch channel is available from two to four. The communication manner is highly flexible by the variable channel number.

[0015] The sampling and holding circuits SHp1 to SHpS and SHt1 to SHtR are connected at their outputs to analog to digital (A/D) converters ADp1 to ADpS and ADt1 to ADtR, respectively. The A/D converters convert the outputs of the

sampling and holding circuits into digital signals. ADp1 to ADpS output the digital signals to a multi-path-signal multi-plexer MUX31, and ADt1 to ADtR output the digital signal to a multi-path-signal multi-plexer MUX32. These multi-plexers output one of outputs from the connected A/D converters for the fading compensation and rake combining in the following circuits in time-sharing manner. The circuits for the fading compensation and rake combining are with small size due to the timesharing. The A/D converters ADp1 to ADpS can be substituted by one A/D converter which is used in the time-sharing manner for converting outputs of the sampling and holding circuits SHp1 to SHpS into digital signals. The A/D converters ARt1 to ADtR can be similarly substituted by one A/D converter.

[0016] MUX31 outputs the correlation outputs as the converted output from the A/D converters of the perch channel to a memory MEM31 for registering the correlation outputs. An in-phase component (I-component) and a quadrature component (Q-component) of the correlation outputs are compensated by a fading compensation circuit PC31 and input to a rake combiner RCM31. The rake combiner RCM31 generates a rake combined output Sout1. MUX32 outputs the correlation peaks of the traffic channel to a memory MEM32 for registering the correlation outputs. An in-phase component (I-component) and a quadrature component (Q-component) of the correlation outputs are compensated by a fading compensation circuit PC32 and input to a rake combiner RCM32. The rake combiner RCM32 generates a rake combined output Sout2.

[0017] Fig.4 is a timing chart of the circuit in Fig.6. Only the processes of the perch channel by MF01 and of the traffic channel by MF21 are shown for easy understanding. When a multi-path signal "Peak01" of three peaks from a base station "a" is received by MF01 of the perch channel in a symbol period, three of the sampling and holding circuits SHp1 to SHpS are used for holding the signal. Here, a multi-path signal of two peaks from another base station "b" occurs. The matched filter MF21 of the traffic channel receives a signal "Peak21" of five peaks, the total peaks of the two base stations above. Five of the sampling and holding circuits SHt1 to SHtR are used for holding the signal. The sampled data in the perch channel is registered in the memory MEM31 as shown by MEM01, and the sampled data in the traffic channel is registered in the memory MEM32 as shown by MEM21. The fading compensation and rake combining are performed for the data registered.

[0018] Since the delay profile of the received signal is not so quickly changed, a delay profile of one symbol period is assumed as a delay profile of the next symbol period. The phase of the multi-path in the traffic channel can be predicted.

[0019] For the soft-handover, the signals from both peripheral base stations and the current base station are to be simultaneously received and processed until the next base station is determined. In Fig.4, the signals from the base stations "a" and "b" are simultaneously received by the matched filter MF21 of the traffic channel. Different spreading codes are used for the base stations "a" and "b", so the spreading codes are alternatively supplied for receiving signals from different base stations.

[0020] As shown in Fig.2, the spreading codes are supplied to the matched filters through two calculation registers CAL-REG1 and CAL-REG2. Input registers INP-REG1 and INP-REG2 are connected to the registers CAL-REG1 and CAL-REG2, respectively. Different spreading codes Pa and Pb are input to the input registers INP-REG1 and INP-REG2, respectively, and transferred to the calculation registers CAL-REG1 and CAL-REG2, respectively CAL-REG1 and CAL-REG2 are shift registers and their last stages are connected to the first stages, respectively. Data in the total stages of the registers CAL-REG1 and CAL-REG2 are parallelly input to phase-multi-plexers PMUX1 and PMUX2, respectively. PMUX1 and PMUX2 output the current data of CAL-REG1 and CAL-REG2, respectively, or the data of one chip time before the current data of CAL-REG1 and CAL-REG2, respectively, to a register-multi-plexer RMUX. The register-multi-plexer RMUX outputs alternatively the data from PMUX1 or PMUX2 as a data MUXCNT.

[0021] As shown in Fig.3, the phase-multi-plexer PMUX1 includes a data-multi-plexer DMUX1 receiving data D1 from the first stage and data D2 from the second stage, a data-multi-plexer DMUX2 receiving data and data D3 from the third stage, ..., a data-multi-plexer DMUXn-1 receiving data Dn-1 from the (n-1)th stage and data Dn from the last nth stage, and a data-multi-plexer DMUXn receiving data Dn and D1 of CAL-REG1. It is possible that signals from different base stations have peaks at the same timing. These peaks have to be separated for one another. When there are no peaks overlapping (normal condition), PMUX1 outputs D1 to Dn as they are. When there are peaks overlapping at the same timing (overlapping condition), one of the two signals is shifted by one chip time. On the overlapping condition, PMUX1 output D2 to Dn and D1, respectively. These are the data of DMUX1 to DMUXn one chip time before. PMUX2 is similar to PMUX1, so the description therefor is omitted. If a multi-plexer of more than two inputs is used, more than two signals overlapping can be separated. Then, not only overlapped signals more than two but also two or more continuous overlapping of peaks can be separated.

[0022] As shown in Fig.1, an additional sampling and holding circuit SHEX receiving the input signal Vin is provided besides sampling and holding circuits SH1 to SHn. A multi-plexer MUXEX is connected to an output of the sampling and holding circuit SHEX. An output of the multiplexer MUXEX is input the "p" and "m" terminals of the adder ADD. In the case that the overlapping of peaks occurs just after SH1 samples Vin, this overlapping is predicted before one symbol period and the signal at the timing of the overlapping is held by both of the SHEX and the SH2. When the calculation of the data in SH1 and the spreading code in CAL-REG1 is finished, next the calculation of the same data the spreading

code CAL-REG2 is performed using data in the SHEX not in the SH2, because the data in the SH2 is newly input at this time.

[0023] If the sampling and holding circuit SHEX were not provided, the correlation calculation by the spreading code in CAL-REG2 includes an error due to the renewal data of SH2. However, the error can be ignored when there are a great many taps (number of multiplications) as in the usual DS-CDMA system. Therefore, a system without SHEX can be practically applied.

[0024] The sampling of the input signal Vin to the SHEX can be performed at the timing when the overlapping occurs. Data in the sampling and holding circuits SH1 to SHn are not renewed until the timing the overlapping does not occur. In this system, it is unnecessary to predict the overlapping before one symbol timing.

[0025] The processing above is described with reference to Fig.4. The matched filter MF01 of the perch channel applies the spreading codes P01,a and P01,b for the base stations "a" and "b" one after another. The correlation peaks of the signal from the base stations "a" and 'b' are detected as shown by Peak01. In the traffic channel, the matched filter MF21 applies the spreading codes Pa and Pb one after another for every symbol periods. In the kth and (k+1)th periods, signal of the base stations "a" and "b" are received. Since the overlapping does not occur in the kth and (k+1)th periods, the total correlation peaks are sampled by the sampling and holding circuits SHt1 to SHtR as shown by S/H in Fig.4. After the (k+1)th period, the peaks overlapping of signals from base stations "a" and "b" occurs at the timing shown by "PP". The peak of "b" is delayed by one chip time so that a new peak "PD" is generated. Then, the overlapping is to be avoided. The sampling and holding circuits sample the correlation peaks generated as shown above. The correlation outputs from MF01 are stored in the memory MEM01, and the correlation outputs from MF21 are stored in the memory MEM21. Then, the fading compensation (PHC01 and PHC21) and the rake combining are performed. The more the additional sampling and holding circuits are, the more the continuous overlapping peaks can be processed. The calculation becomes more accurate. When the number of continuous overlapping peaks is "d", data before {(1 symbol period)-(1 chip time)}, data before {(1 symbol period)-(2 chip time)}, ..., data before {(1 symbol period)-(d-1 chip time)} are successively stored so as to generate correlation peaks using the successive data.

[0026] As mentioned above, when the number of continuous overlapping peaks is small relative to the total taps, the additional sampling and holding circuits can be omitted. By alternating the registers CAL-REG1 and CAL-REG2 every chip time, the calculation error is at most an order of one input data.

[0027] A matched filter in Fig.5 can be used. The sampling and holding circuits SHA1 to SHAn are serially connected for transferring data from SHA1, SHA2, ..., SHAn, successively. The input signal Vin is input to SHA1 and an additional sampling and holding circuit SHAEX is connected to an output of SHn. Each of the multi-plexers SMUX1 to SMUXn has two inputs and one output for receiving outputs of adjacent two sampling and holding circuits SHA1 and SHA2, SHA2 and SHA3, ..., SHAn-2 and SHAn-1 and SHAn-1 and SHAn. The first multi-plexer SMUX1 outputs one of the outputs of SHA1 and SHA2, and the kth multi-plexer SMUXk outputs one of the outputs of SHAk and SHAk+1. The outputs of the multi-plexers SMUX1 to SMUXn are input to multi-plexers MUX to MUXn, respectively, which are similar to MUX1 to MUXn in Fig. 1. The outputs of each of multi-plexers MUX1 to MEXn are input to a plus terminal "p" and a minus terminal "m" of an adder ADD. An output of the adder ADD is input to a scaling circuit SCALER for scaling the output of the adder to be an adequate level. An output Vout is generated after the scaling. The multi-plexers MUX1 to MUXn are switched by spreading codes ml to mn, respectively.

[0028] By the connection of SHA1 to SHAn with MUX1 to MUXn, respectively, the correlation peak is calculated of spreading code in CAL-REG1. Then, the connection is shifted to the connection of SHA2 to SHAEX with MUX1 to MUXn, respectively, the correlation peak is calculated of spreading code in CAL-REG2. The connection is then returned to the first.

[0029] Similarly to the above, the additional sampling and holding circuit SHAEX can be deleted if the number of taps is large, and a plurality of additional sampling and holding circuits can be provided for continuous overlapping peaks.

[0030] Fig.7 shows the second embodiment wherein the process of the matched filter MF01 in the first embodiment is performed by the matched filter MF21, while the process of the matched filter MF21 in the first embodiment is performed by a matched filter MF22 in the traffic channel. MF21 applies the spreading codes Pa and Pb of the base stations "a" and "b" alternatively in every symbol periods, MF22 applies Pa and Pb for the correlation peaks to be generated. The processes thereafter are similar to those m the first embodiment, so the description therefor is omitted. As in the second embodiment, the soft-handover can be performed by only the matched filters of the traffic channel.

[0031] Fig.8 shows the third embodiment. The soft-handover is performed only by one matched filter MF21 in the traffic channel. MF21 applies the spreading code Pa at the kth symbol period. In the (k+1)th and (k+2)th symbol periods, the spreading code Pb is used for searching peaks by Pb at the intervals between peaks using spreading code Pa. Then, the correlation peaks of both base stations can be detected. In the (k+3)th period, both spreading codes Pa and Pb are applied.

[0032] Fig.9 is a flowchart of the processing in Fig.8. At the step S1, the peripheral cell search is performed. When it is judged that the soft-handover is necessary according to the peripheral cell search at step S2, candidates BNC1 to BNCn of base stations are determined at step S3. A loop counter "i" is initialized at step S4. The correlation for BNCi is

calculated at the intervals between adjacent peaks of the current base station at step S5. Here, peaks are assumed as Pc1 to Pcm. When a peak is detected (step S6), the position (phase) of the peak is registered at step S8. Even when no peak exists, there is a possibility that the peak overlapping occurs. The correlation timings of Pc1 to Pcm are delayed at step S7, the first peak detected is registered as a correlation peak of the base station BNCi. Then, by changing "i" successively (step S12), correlation peaks of other base stations are searched at step S5. When the peak search of the total base stations is finished (step S1O), a new base stations BN1 to BNp are determined at step S14. After a diversity hand-over (step S15), recursive integration and electrical power calculation is performed, and one base station is selected at step S16.

[0033] As shown in Fig.20, the multi-plexer MUX1 includes a pair of multi-plexers MUX91 and MUX92. The multi-plexer MUX91 includes a pair of CMOS switches T911 and T912 connected to an input voltage Vin9 and the reference voltage Vref, respectively. The multi-plexer MUX92 includes a pair of CMOS switches T912 and T922 connected to the input voltage Vin9 and the reference voltage Vref, respectively. MUX91 and MUX92 are controlled by a control signal Pct which is input to gates of nMOS of T911, pMOS of T912, nMOS of T921 and pMOS of T922. An inversion of Pct is generated by an inverter I9 to be input to gates of pMOS of T911, nMOS of T912, pMOS of T921 and nMOS of T922. When Pct is high level, an output Vout201 of MUX91 is Vin9 and an output Vout202 of MUX92 is Vref. When Pct is low level, the output Vout201 is Vref and the output Vout202 is Vin9. Other multi-plexers MUX2 to MUXn are similar to MUX1, so descriptions therefor are omitted.

[0034] Fig.21 shows a variation of the multi-plexer MUX1. In Fig.21, similar portions to those in Fig.20 are designated by the same references. There are two control signals Pct1 and Pct2, the former controls the switches T911 and T922, and the latter controls the switches T912 and T921. The control signals Pct1 and Pct2 are generated by a pre-control signal Pct. Pct is delayed by two stages buffers B91 and B92 and input to a NOR-gate G91 so that Pct1 is generated. The output of the buffer is also input to an AND-gate G92 so that Pct2 is generated. The control signals Pct1 and Pct2 become low level without fail in the time distance from the trailing edge of Pct1 to the leading edge of Pct2 and in the time distance from the trailing edge of Pct2 to the leading edge of Pct1. It means that Vin9 and Vref are never simultaneously output. Even when the spreading codes are quickly switched the outputs of the multi-plexers are stable. The reference voltage Vref is not influenced by unstable outputs of the multi-plexers.

[0035] In Fig.22, the sampling and holding circuit SH1 includes a switch SW43 connected to an input signal Vi4 (corresponding to Vin in Fig. 1), an input capacitance C42 connected to the switch SW43, an inverting amplifier INV4 consisting of CMOS connected to the input capacitance C42 and a feedback capacitance C41 for connecting an output of the inverting amplifier INV4 to its input. When the switch SW43 is changed from closed to opened, Vi4 (Vin) is held. A refresh switch SW42 is connected to INV4 parallelly to C41, and a refresh switch SW44 is connected to C42 for connecting a reference voltage to an input of SW44. The reference voltage is equal to a threshold voltage of INV4, and the input of INV4 is substantially the threshold voltage constantly. When SW42 is closed, the opposite terminals of C42 become the equal voltage and an electrical charge of C42 is deleted. A switch SW41 connected to a ground is connected to the input of INV4. When SW41 is closed, INV4 is connected to the ground at the input so that a CMOS included in INV4 becomes saturated condition. The electrical power consumption is stopped. The other sampling and holding circuits are similar to SH1, so the description therefor is omitted.

[0036] While, the sampling and holding circuit SHA1 consists of two of the sampling and holding circuit in Fig.22, which are serially connected through a switch. The description therefor is omitted.

[0037] As shown in Fig.23, the switch SW43 includes a transistor circuit T5 having pMOS and nMOS parallelly connected to an input voltage Vin5. A dummy transistor circuit DT5 is connected to an output of the transistor circuit T5. The dummy transistor circuit DT5 includes pMOS and nMOS parallelly connected to output of the transistor circuit T5, inputs and outputs of pMOS and nMOS are short-circuited. A clock CLK0 is input to gates of n-MOS of T5 and pMOS of DT5, and an inversion of CLK0 is input to gates of pMOS of T5 and nMOS of DT5. The inversion is generated by an inverter I5. The other switches are similar to SW43, so description therefor is omitted.

[0038] As shown in Fig.24, the adder ADD includes capacitances Cp1 to Cpn and Cm1 to Cmn for the plus terminals "p" and minus terminals "in" in Fig. 1, respectively. Outputs of Cp1 to Cpn are commonly connected to an input of an inverting amplifier INV71. Outputs of Cm1 to Cmn are commonly connected to an input of an inverting amplifier INV72. An output of INV71 is connected through a feedback capacitance CF71 to its input. An output of INV72 is connected through a feedback capacitance CF72 to its input. The output of INV71 is connected through an intermediate capacitance CC7 to the input of INV72. The adder can perform addition and subtraction. When the capacity ratios of Cp1 to Cpn, Cm1 to Cmn, CC7, CF71 and CF72 are as in the formula (1), the output voltage Vout6 is given as in the formula (2).

$$CM1 = CM2 = \ldots = Cmn = Cp1 = Cp2 = \ldots = Cpn = \frac{CF71}{n} = \frac{CC7}{n} = \frac{CF72}{n} \quad (1)$$

$$Vout4 - Vb = Vdd - \frac{\sum_{i=1}^{n} Vo1ip - \sum_{i=1}^{n} Vo1im}{n} \quad (2)$$

[0039] Fig. 10 shows the second embodiment of the present invention for multi-code processing. In the perch channel, the received signal (control signal) is despread by the matched filter MF01 with a spreading code PNP, while in the traffic channel, a multi-code despread by the matched filter MF21 with spreading codes PNT1 and PNT2 is performed. The matched filters MF01 and MF21 perform the path search and signal reception. When the spreading ratios of the perch channel and the traffic channel are equal to each other, the path patterns of both channels are equal as shown by Peak01 and Peak21. in Fig.4. Peak01 shows the path pattern in the perch channel and Peak21 shows the path pattern in the traffic channel. Since the path pattern of the traffic channel is determined from the path pattern of the perch channel, the path search in the traffic channel can be omitted. Higher peaks are selected from the peaks detected in the traffic channel. When three peaks shown by solid lines in Peak21 of a multi-path signal are selected by the despread of MF21 with PNT1 in a symbol period, multipath peaks by PNT2 shown by broken lines in Peak21. The peaks of PNT2 are separated by delaying the timing of the despread, then six peaks are generated. These peaks are sampled and held by six of the sampling and holding circuits SHt1 to SHtR as shown in S/H in Fig.4. The sampled peaks are then stored in the memory MEM01 The fading compensation and rake combining are performed for the stored data. The processing by MF01 in the perch channel is similar to the above, so the description therefor is omitted.

[0040] Fig. 14 shows another embodiment of the multi-code processing. Only one matched filter MF21 is used for the processing of two spreading codes PNt1 and PNt2. The output of the matched filters are used as an information signals after stored for a predetermined time length as mentioned. above. It is possible to calculate the electrical power from the output and to perform path search from the power. It is also possible to change the process in response to change in the path pattern. The correlation peaks are held by some of the sampling and holding circuits SHt1 to SHtR and stored in the memory MEM21 similarly of the above.

[0041] Figs. 11 to 13 are flowchart of the processing in Fig. 14. As shown in Fig. 11, the path pattern is determined from the path selection at step S71, then the reception schedule is determined at step 72. The signal is received according to this schedule at step S73. In scheduling, the number of the additional sampling and holding circuits, number of spreading codes and time length of one symbol period are judged. Here, the number of the additional sampling and holding circuits is SSH, the number of spreading codes is CN, time length of one symbol period is Symbol, the number of peaks is Pmax, time distances between adjacent peaks are Dj. A plurality of groups of peaks are defined, each consisting of peaks of distances Dj<(CN-1). Each group is defined by a number PG and the number of peaks consisted in each group is defined as PNG(PG).

[0042] As shown in Fig. 12, a timing number "i", a loop counter "j" of repetition for each group, the PG and the Pmax are initialized at step S801. A correlation is calculated by a spreading code PNS I at the timing "i", (step S802). The correlation result is defined as CR(i). When CR(i) is equal to or higher than a predetermined threshold θ, it is judged that a correlation peak occurs at this timing (step S804). When this peak is the first detected (step S806), Pmax is increased by one (step S805). The timing "i" is also increased by one (step 803).

[0043] When two or more peaks are detected, the time distance Dj between each peak and the next peak ahead is evaluated (step S807). When Dj is equal to or longer than (CN-1) and the timing is not at the end of the symbol period (step S810), this peak is classified in to another group than a group including peaks before the peak (step S811). When Dj is smaller than (CN-1), it is judged whether the number of the additional sampling and holding circuits is sufficient for processing the peaks as one group or not (step S808). If possible, the counter "j" and the number of peaks PNG(PG) in the group are increased by one. When the number of the additional sampling and holding circuits is insufficient, the timing "i" is increased by one (step S803) and the next correlation is calculated step (S802). Correlation peaks in one group are processed by holding signals in the additional sampling and holding circuits so that the same signal is processed by different spreading codes.

[0044] An evaluation of the formula (3) is performed (step S808). If SSH is greater or equal to the right side in the formula (3), the peaks are processed. While if SSH is not bigger, peaks of a number TP not bigger than SSH are processed and the rest of peaks are neglected.

$$SSH \geq (CN\text{-}1) \cdot j - \sum_{j=1}^{PGN(PG)-1} \quad (3)$$

[0045] As shown in Fig. 13, the numbers PG and TP are initialized (step S91) at the signal reception step S73. The counter "j", a number "k" of the spreading code and a delay time "d" are initialized (step S92). A correlation is calculated

by a spreading code PNSk at the delay time "d" (step S93). This process continues until "j" reach PGN(PG) (step S94). When j is smaller than PGN(PG), d, j and k are increased by one and the correlation calculations are repeated. When j becomes equal to PGN(PG), TP is increased by PGN(PG) (step S96). If the TP does not reach Pmax, PG is increased by one so that a new group of peaks begins (steps S98 and S92).

[0046] Fig. 15 is a timing chart of the third embodiment of processing for long-delay signals. In a symbol period, matched filters MF01, MF02, MF11 and MF12 in the perch channel receive the signal. When five peaks of multi-path signal occurs as shown by Peaks in Fig. 15 in one of the matched filters, five of the sampling and holding circuits SHp1 to SHpS are used for sampling as shown by S/H. The sampled data are stored in the memory MEM31 as shown by "memory". Then, the fading compensation and rake combining are performed.

[0047] When a long-delay signals occurs in the traffic channel, that is, a multi-path signal including a signal delaying more than one symbol period, this delay signal can usually be detected in the perch channel because the symbol period of the perch channel is longer than, such as twice as long as, the symbol period of the traffic channel. If the symbol period of the perch channel is twice as long as the symbol period of the traffic channel, the peaks in the latter half of the symbol period of the perch channel are long-delay paths in the traffic channel. The delay profile is not steeply changed, the delay-profile is applied to the next symbol period. Therefore, the multipath phase in the traffic channel can be predicted.

[0048] As shown in Fig. 16, the spreading codes are supplied to the matched filters from two sets of calculation registers CAL-REG and LDPREG. The current spreading code is stored in CAL-REG and a spreading code one symbol period before the current sequence is stored in LDP-REG. Parallel outputs of CAL-REG and LDP-REG are input to a register-multiplexer RMUX for alternatively outputting one of the parallel outputs as a control signal MUCCNT. The control signal MUXCNT are input to the multi-plexers MUX1 to MUXn in Fig. 1 for controlling them. Since a new spreading code must be loaded into CAL-REG instantaneously just after the end of one symbol period, the new sequence is advantageously loaded into an input register INP-REG during the last symbol period. The sequence in INP-REG is parallelly transferred to CAL-REG. Just before the parallel transfer from INP-REG to CAL-REG. The sequence in CALREG is transferred to LDP-REG so that the sequence one symbol period before is stored in LDP-REG. The multi-plexer RMUX supplies the current spreading code in CAL-REG to the matched filters for not long-delay signal and supplies the spreading code one period before in LDP-REG to the matched filter for the long-delay signal. Therefore, long-delay path can be detected by one matched filter. The circuit of the signal reception apparatus is small. When two or more long-delay registers LDP-PEG are used, signals delaying by two symbol periods or more can be detected.

[0049] It is possible that a multi-path and long-delay path occurs at the same time in one matched filter. The long-delay register receives clocks CK1, CK2 and a ground voltage GND at its clock input through a multiplexer CMUX CK1 is synchronous to the sampling timing of the sampling and holding circuits, and CK2 is a clock much quicker than, such as four times as, CK1. At the timing when the correlation peaks occurs simultaneously, the current spreading code in CAL-REG is supplied through RMUX to the matched filters and the spreading code in LDP-REG is not used. At this time, CMUX is changed to GND so that the circulated shifting of LDP-REG is stopped. At the next timing, LDP-REG is selected so that the correlation is calculated by the sequence in LDP-REG one symbol period later. The overlapping peaks are separated and detected.

[0050] As shown in Fig. 17, the matched filter MF01 in the perch channel has finished kth correlation calculation and simultaneously the matched filter MF21 in the traffic channel has finished the kth and (k+1)th correlation calculation. The spreading codes PN01 and PN21 are applied to the matched filters MF01 and MF21, respectively. In the kth period, a spreading code PO1,k of PN01 is applied to MF01 in the perch channel. In the kth and (k+1)th periods, spreading codes Pk and Pk+1 of PN21 are applied to MF21 in the traffic channel.

[0051] When correlation peaks occur in the lab period as shown in Peak01, the peaks in the latter half of the lab period are long-delaying paths. Peaks in the traffic channel corresponding to these long-delaying paths of the perch channel are shown by broken lines in the kth period in Peaks21. In the kth period, there no peak overlapping, so the total peaks are held by the sampling and holding circuits SHt1 to SHtR following to the matched filters as shown in S/H. The long-delay path can be detected by this process. In the (k+3)th period of MF21, the peak overlapping occurs by the current spreading code and the log-delay spreading code at the timing shown by PP in Peaks21. The long-delay correlation is delayed as mentioned above, the long-delay peaks are generated in a delayed timing as shown by PD, then the overlapping is prevented. The sampling and holding circuits hold the peaks above. The correlation outputs of MF01 and MF21 are stored in the memories MEM01 and MEM21, respectively. Similarly to the process in Fig. 15, the fading compensation (PHC01 and PHC21) and rake combining are executed.

[0052] The more the additional sampling and holding circuits are, the more the continuous overlapping peaks can be processed. The calculation becomes more accurate. When the number of continuous overlapping peaks is "d", data before {(1 symbol period)-(1 chip time)}, data before f {(1 symbol period)-(2 chip time)}, ..., data before {(1 symbol period)-(d-1 chip time)} are successively stored so as to generate correlation peaks of long-delay paths using the successive data. Then, (d+1) times circulated shifting is quickly performed for LDP-REG within on chip time so as to take LDP-REG up of the required state.

[0053] In Fig. 18, another circuit for long-delay path is shown. In the figure, similar portions to those in Fig. 16 is designated by the same references. A sub-long-delay register SUB-LDP-REG is provided for storing the same spreading code as that in LDP-REG, with shifted to be delayed by one chip time than that in LDP-REG. Instead of the stop of shifting in the circuit of Fig. 16, RMUX is switched to SUB-LDP-REG for outputting the spreading code delayed by one chip time. This is equivalent to the process by the stop of the shifting. Then RMUX is returned to LDP-REG so that the process is returned to the condition of no peak overlapping. A clock CK is input through a gate G to SUB-LDP-REG. The clock can be stopped by G during one chip time. Then, the circulated shifting is delayed by one chip time. This circuit does not need high speed clock used in the circuit of Fig. 16. This circuit is advantageous for rather low speed circuit and the circuit size is small.

[0054] When a plurality of peak-overlappings occur continuously, a plurality of sub-long-delay registers SUB-LDP-REG successively delayed by one chip time are used. The number of SUB-LDP-REG is equal to the number of peak-overlappings. Similarly to the circuit of Fig. 16, by using CAL-REG and LDP-REG one after another, only one SUB-LDP-REG and only one SHEX are necessary.

[0055] Fig. 19 shows further another circuit for log-delay path. In the figure, similar portions to those in Fig. 16 is designated by the same references. One clock CK is commonly input to INP-REG, CAL-REG and LDP-REG. The stages of CAL-REG and LDP-REG are fed back to their first stages. The data in LDP-REG are input to a phase-multi-plexer PMUX1 and the data in CAL-REG are input to a phase-multi-plexer PMUX2. PMUX1 and PMUX2 output the data in LDP-REG and CAL-REG as they are or delayed by one chip time. Outputs of PMUX1 and PMUX2 are input to a register multi-plexer RMUX which alternatively outputs the outputs of CAL-REG or LDP-REG.

Claims

1. A signal reception apparatus for direct sequence code division multiple access (DS-CDMA) cellular system comprising:

   a set of a plurality of sampling and holding circuits for holding an input signal successively input:
   a plurality of matched filters each for calculating a correlation every predetermined periods (symbol periods) between said input signal held by said sampling and holding circuits and a spreading code sequence, said spreading code sequence being a sequence of composite code of a long code indicating a base station and a short code indicating a mobile station;
   a plurality of calculation registers for supplying said spreading code sequences to said matched filters, said calculation registers being classified into a plurality of groups corresponding to said matched filters, each said group including one or more of said calculation registers; and
   a multi-plexer means provided for said groups including a plurality of calculation registers for selectively connecting one of said calculating registers in each said group to said corresponding matched filter.

2. A signal reception apparatus as claimed in Claims 1, wherein said set of sampling and holding circuits are parallelly connected to said input signal and are controlled so that said input signal is held by said sampling and holding circuits one after another on every chip time, and said spreading code sequences are circulatively shifted in said calculation registers synchronous to said sampling timing.

3. A signal reception apparatus as claimed in Claims 2, wherein said set of sampling and holding circuits comprises sampling and holding circuits serially connected from a first stage to a last stage and said spreading code sequence is transferred in a direction from said first stage to said last stage.

4. A signal reception apparatus as claimed in Claims 2, further comprising a phase-multi-plexer connected between said calculation registers and said multi-plexer means for selectively outputting said spreading code sequence of a shifting condition at that time or of a shifting condition before said condition, whereby said spreading code sequences of different calculation registers at a same timing are successively supplied to said matched filter so that correlation peaks at a same time by different spreading code sequences are separately generated.

5. A signal reception apparatus as claimed in Claims 2, further comprising one or more additional sampling and holding circuits for holding said input signal at a timing of {(one symbol period) - (one chip time)} before a time when correlation peaks occur by different spreading code sequences and at intervals of (one chip time) before and from said timing of {(one symbol period) - (one chip time)} before said timing.

6. A signal reception apparatus as claimed in Claims 2, further comprising one or more additional sampling and holding circuits for holding said input signal at a time when correlation peaks occur by different spreading code

sequences and at timings at intervals of (one chip time) after and from said time.

7. A signal reception apparatus as claimed in Claims 1, wherein one of said matched filters is allocated to a perch channel and one to a traffic channel and said matched filter allocated to said perch channel performs a path search for finding a timing when said matched filter allocated to said traffic channel is to calculate correlation.

8. A signal reception apparatus as claimed in Claims 1, wherein one of said matched filters is allocated to a traffic channel which performs a path search for finding a timing to calculate correlation by changing said spreading code sequences every said symbol periods, thereafter performs correlation calculation by itself.

9. A signal reception apparatus as claimed in Claims 1, further comprising a selector means connected between said sampling and holding circuits and said calculation register for keeping a relationship between said sampling and holding circuits and said spreading code sequence in said calculation register unchanged, said multi-plexer means being switched for calculating correlation by different spreading code sequences with input signal in said sampling and holding circuits with keeping said relationship between said sampling and holding circuits and said spreading code sequence in said calculation register unchanged, said selector means returned thereafter to a condition before keeping said relationship unchanged, whereby said peaks are separately generated.

10. A signal reception apparatus as claimed in Claims 9, wherein, when said peaks by different spreading code sequences continuously occur at a plurality of timings, said selector means keeps said relationship between said sampling and holding circuits and said spreading code sequence in said calculation register unchanged during said plurality of timings, whereby said plurality of peaks separately generated.

11. A signal reception apparatus as claimed in Claims 5, wherein, when a correlation peak occurs after a correlation peak in one symbol period and a time distance between said successive peaks is equal to or more than CN • Tt, where CN is a number of spreading code sequences and Tt is a chip time, said correlations by said total spreading code sequences are successively calculated during said time distance, and when a correlation peak occurs after a correlation peak in one symbol period and a time distance between said successive peaks is less than CN • Tt, said correlation by one of said spreading code sequence is calculated duaring said time distance and then correlations by other spreading codes are calculated thereafter.

12. A signal reception apparatus as claimed in Claims 11, wherein, when a plurality of correlation peaks occur in one symbol period and a formula (C1) is true, where SSH is a number of said additional sampling and holding circuits, CP is a number of correlation peaks with shorter distance than (CN • Tt) between successive peaks and D_{k+1} is a distance between kth peak and (k+1)th peak,

$$SSH < (CN - 1) \cdot CP - \sum_{i=2}^{CP} D_i \qquad \text{(C1)}$$

correlation calculations for peaks of number of PP in a formula (C2) are executed and correlation calculations for peaks of number of (CP-PP) are omitted.

13. A signal reception apparatus as claimed in Claims 1 to 12, wherein said plurality of calculation registers of one group hold spreading code sequences of a plurality of base stations for soft-handover.

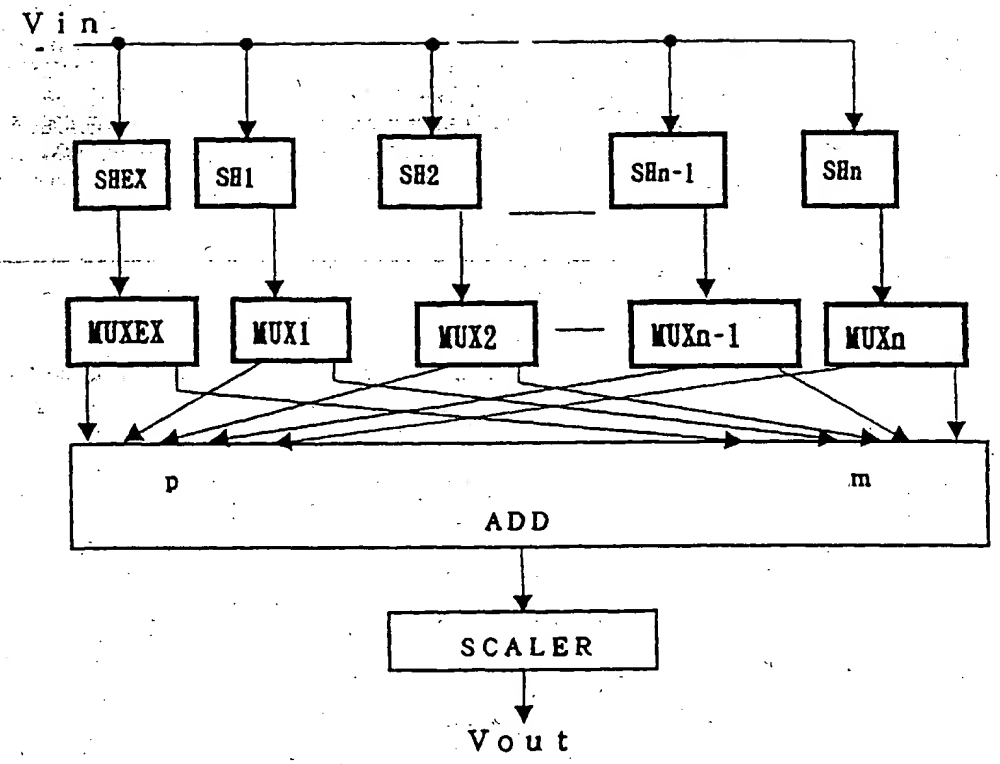
14. A signal reception apparatus as claimed in Claims 1 to 12, wherein said plurality of calculation registers of one group hold a plurality of different spreading code sequences for multi-code processing.

15. A signal reception apparatus as claimed in Claims 1 to 12, wherein said plurality of calculation registers of one group hold a spreading code sequence with a delay within one symbol period and a spreading code sequence with a delay over one symbol period.

16. A signal reception apparatus as claimed in Claim 15, wherein one or more of said symbol periods for one or more of said matched filters are longer than said symbol period for another of said matched filters, whereby said former can detect a correlation peak of said latter delayed more than said symbol period of said latter.

17. A signal reception apparatus as claimed in Claim 16, wherein said former is allocated to a perch channel and said latter is allocated to a traffic channel.

Fig.1


Vin
SHEX
SH1
SH2
SHn-1
SHn
MUXEX
MUX1
MUX2
MUXn-1
MUXn
p
m
ADD
SCALER
Vout

EP 0 932 262 A2

Fig.2

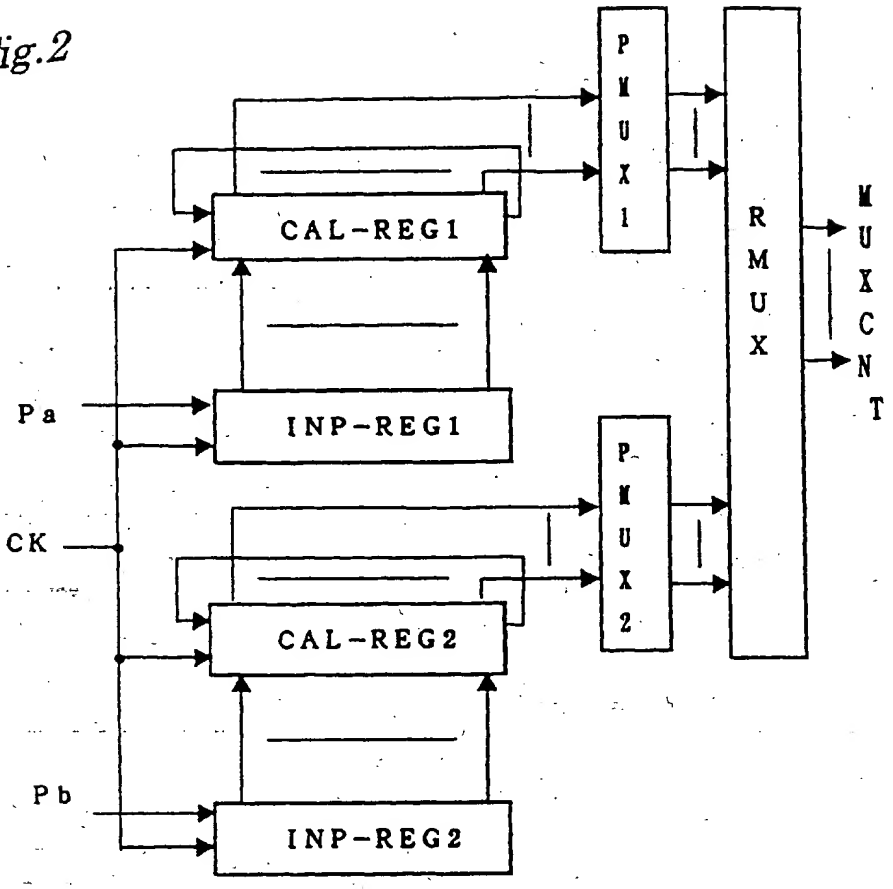


Fig.3

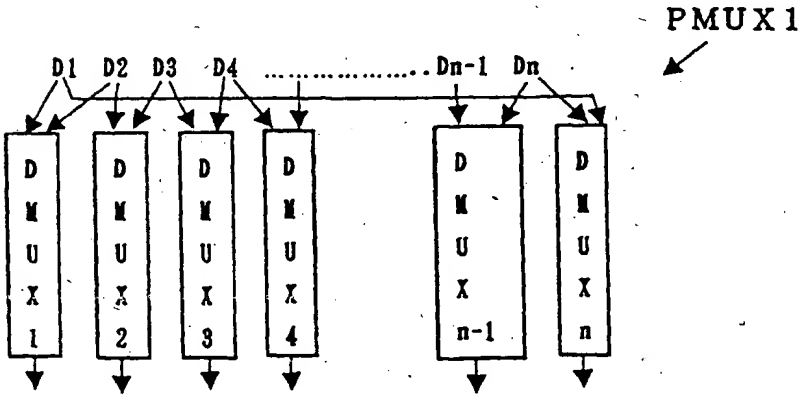
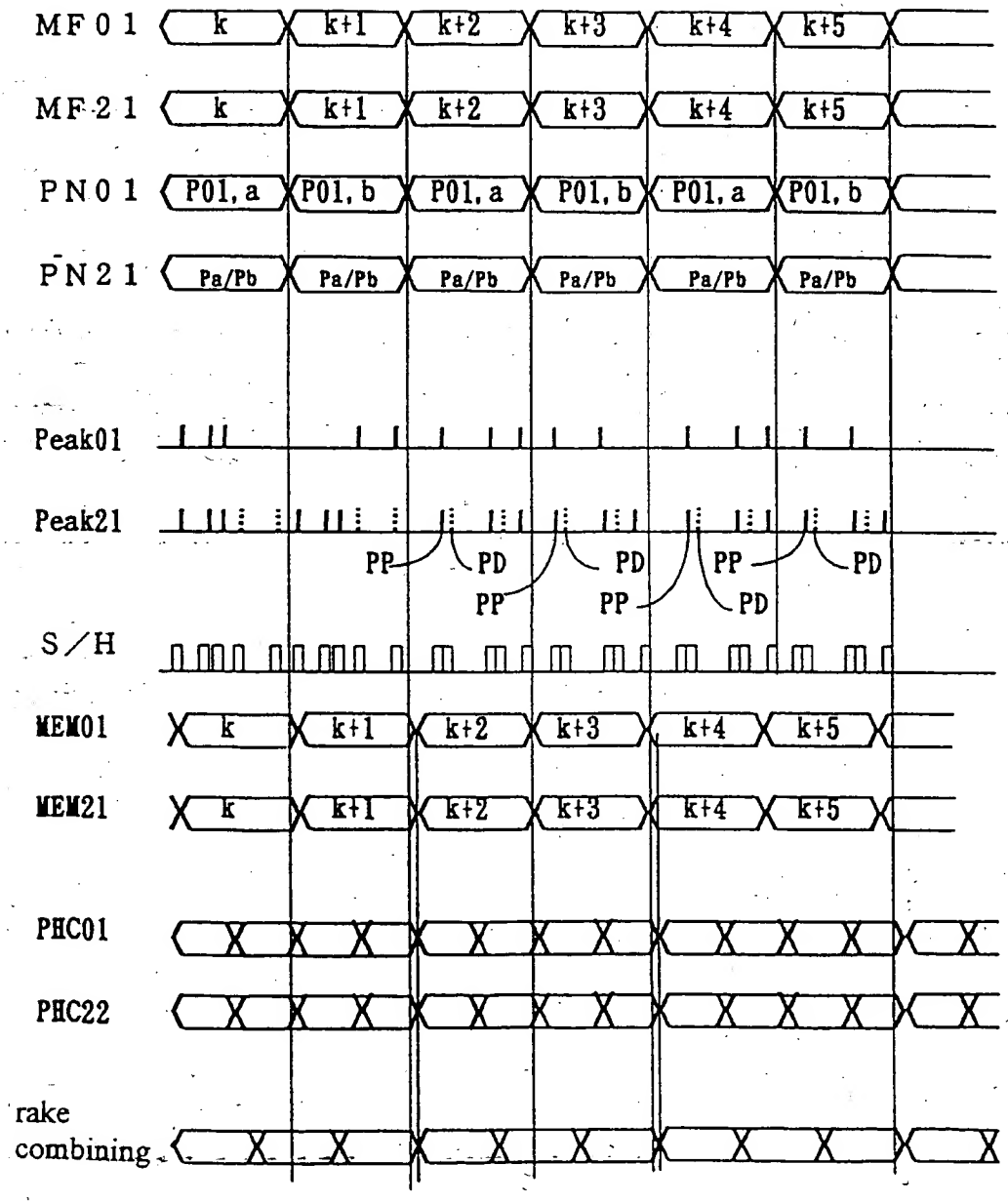
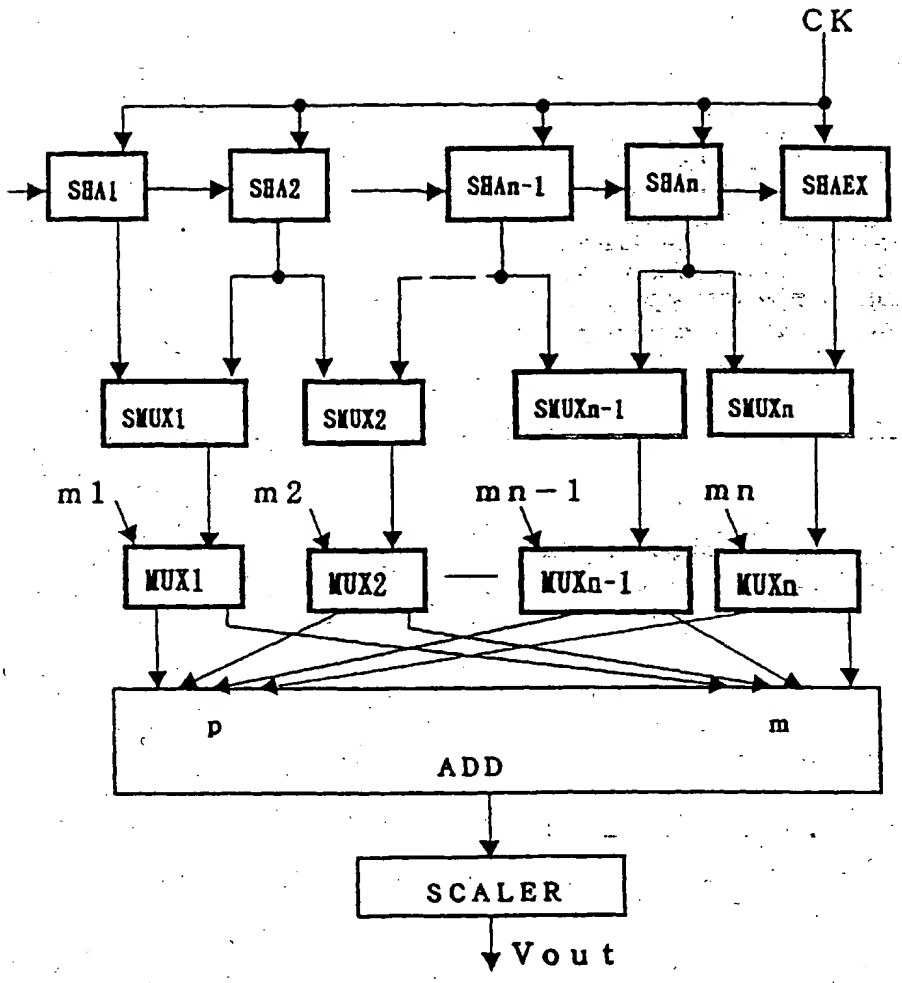


Fig.4


MF01
MF21
PN01
PN21
Peak01
Peak21
S/H
MEM01
MEM21
PHC01
PHC22
rake combining
k
k+1
k+2
k+3
k+4
k+5
P01,a
P01,b
Pa/Pb
PP
PD

EP 0 932 262 A2

Fig.5



EP 0 932 262 A2

Fig. 6

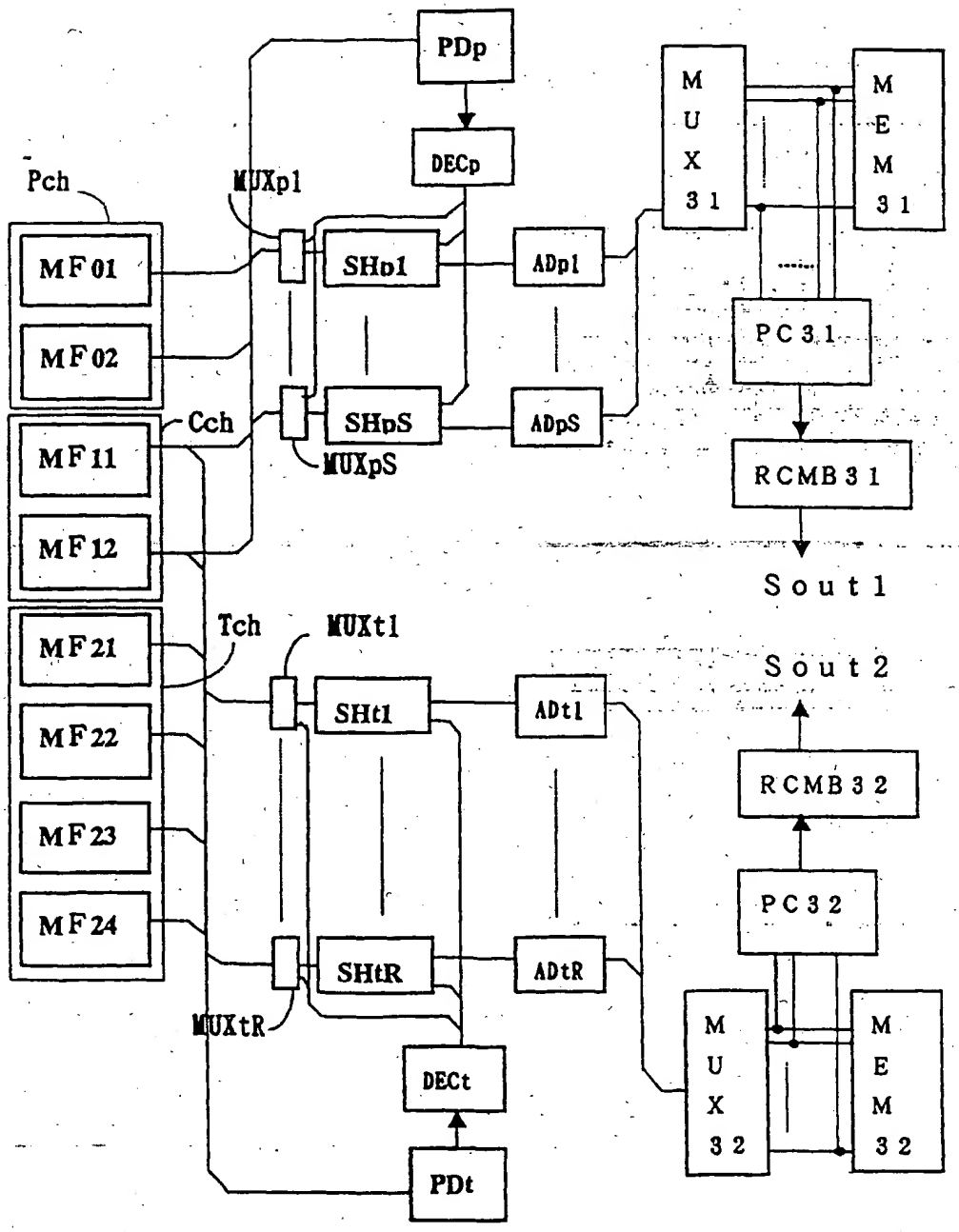


Fig. 7

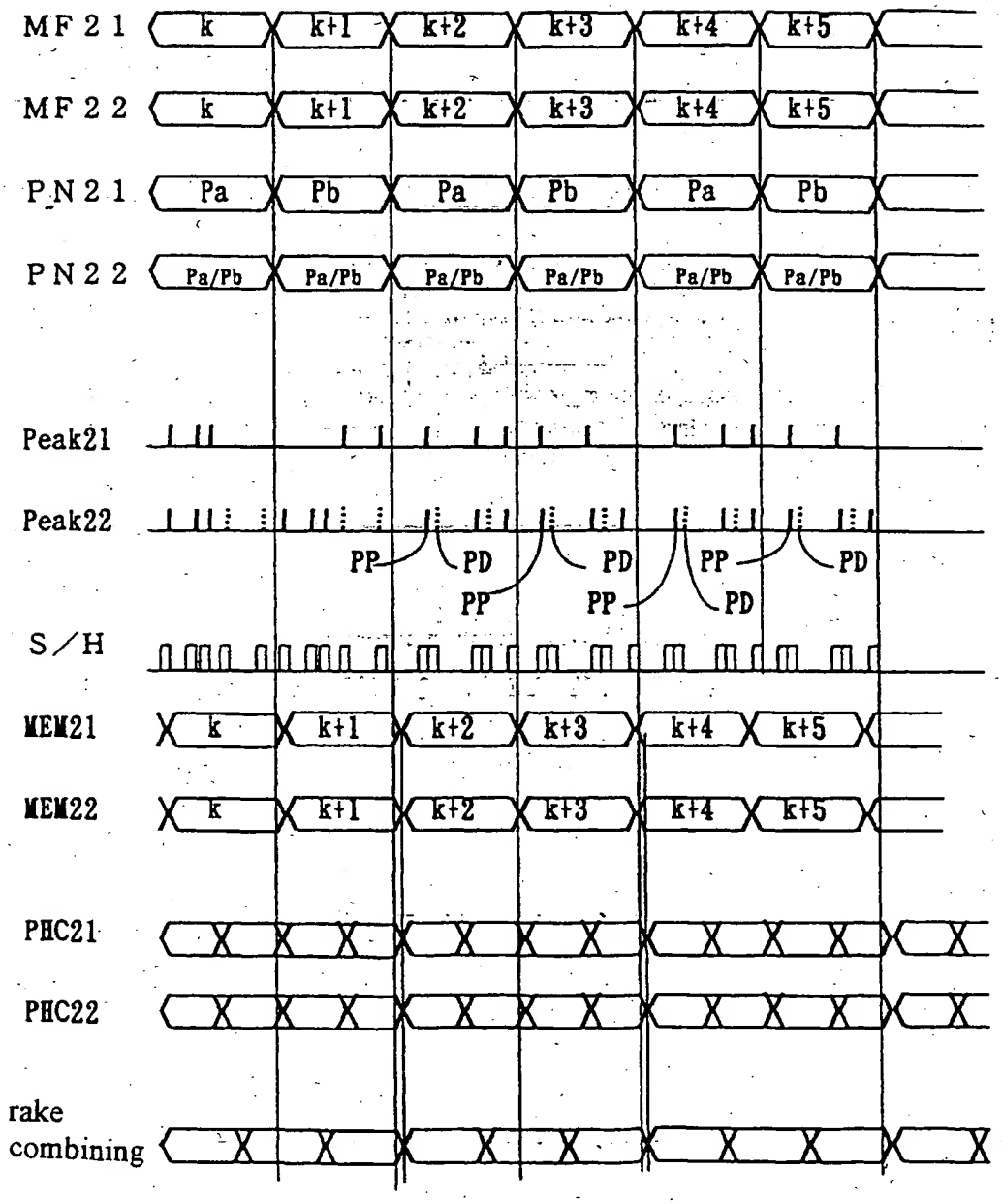

MF 2 1
MF 2 2
PN 2 1
PN 2 2
Peak21
Peak22
S/H
MEM21
MEM22
PHC21
PHC22
rake combining
k
k+1
k+2
k+3
k+4
k+5
Pa
Pb
Pa/Pb
PP
PD

Fig.8

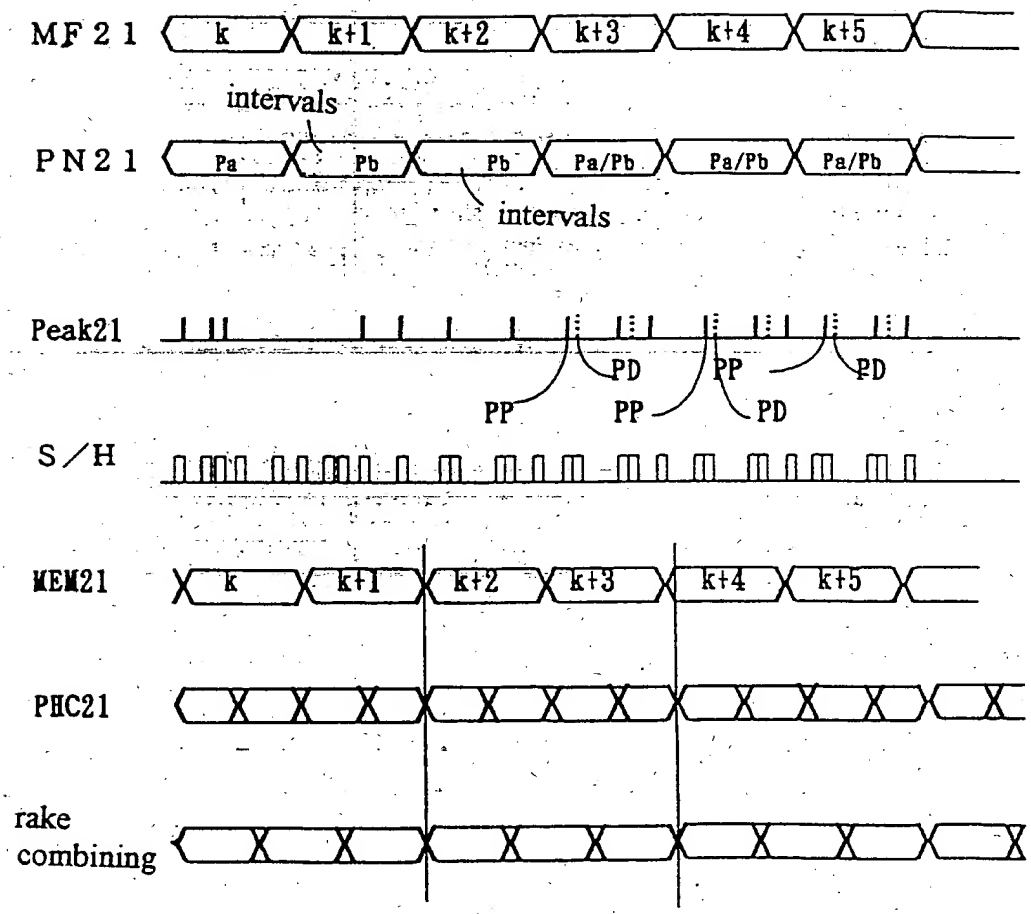

MF21
k
k+1
k+2
k+3
k+4
k+5
intervals
PN21
Pa
Pb
Pb
Pa/Pb
Pa/Pb
Pa/Pb
intervals
Peak21
PP
PD
PP
PD
PP
PD
S/H
MEM21
k
k+1
k+2
k+3
k+4
k+5
PHC21
rake
combining

Fig.9

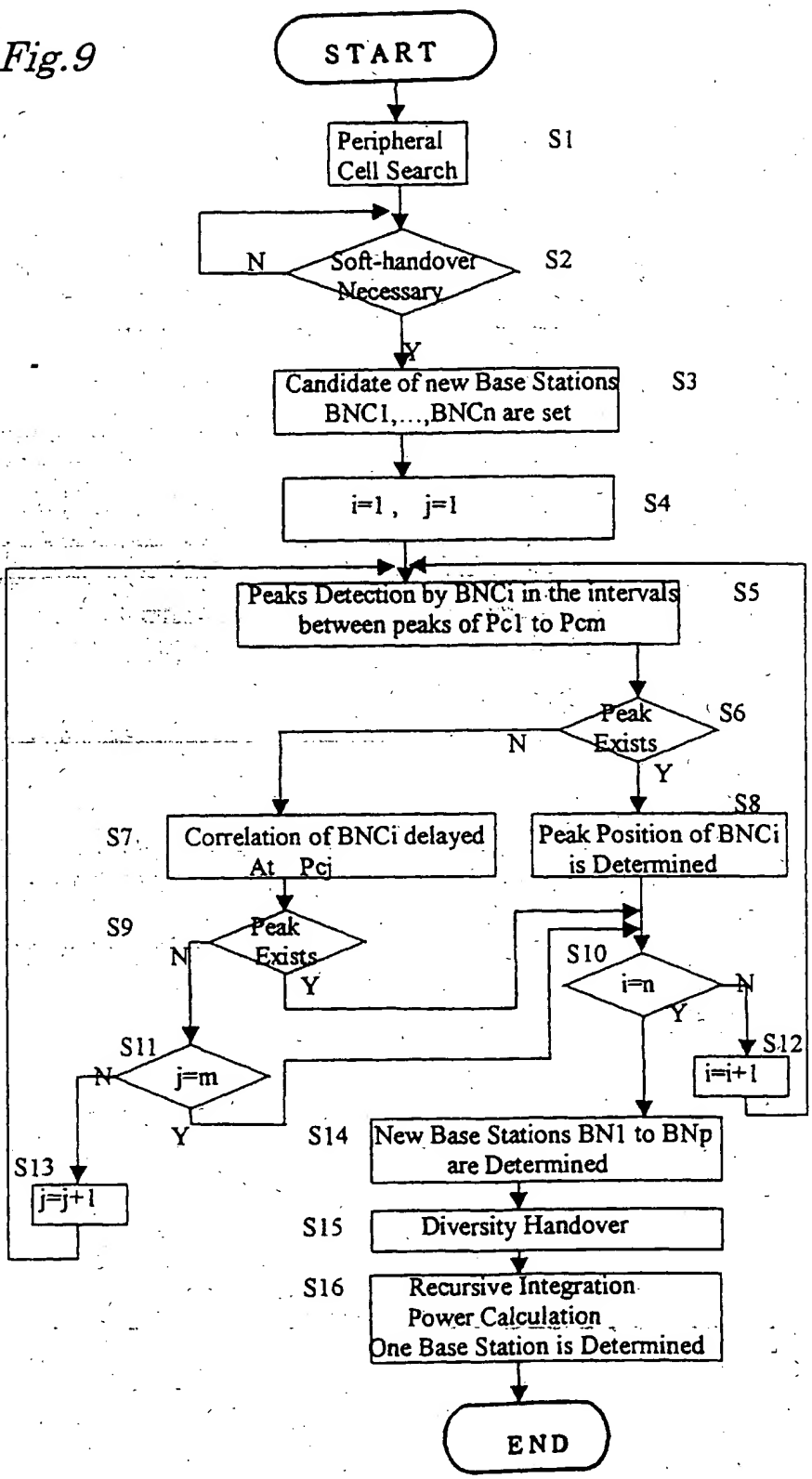

START
Peripheral Cell Search
S1
N
Soft-handover Necessary
S2
Y
Candidate of new Base Stations BNC1,...,BNCn are set
S3
i=1 , j=1
S4
Peaks Detection by BNCi in the intervals between peaks of Pc1 to Pcm
S5
Peak Exists
S6
N
Y
S7
Correlation of BNCi delayed At Pcj
S8
Peak Position of BNCi is Determined
S9
Peak Exists
N
Y
S10
i=n
N
Y
S11
j=m
N
Y
S12
i=i+1
S13
j=j+1
S14
New Base Stations BN1 to BNp are Determined
S15
Diversity Handover
S16
Recursive Integration Power Calculation One Base Station is Determined
END

Fig.10

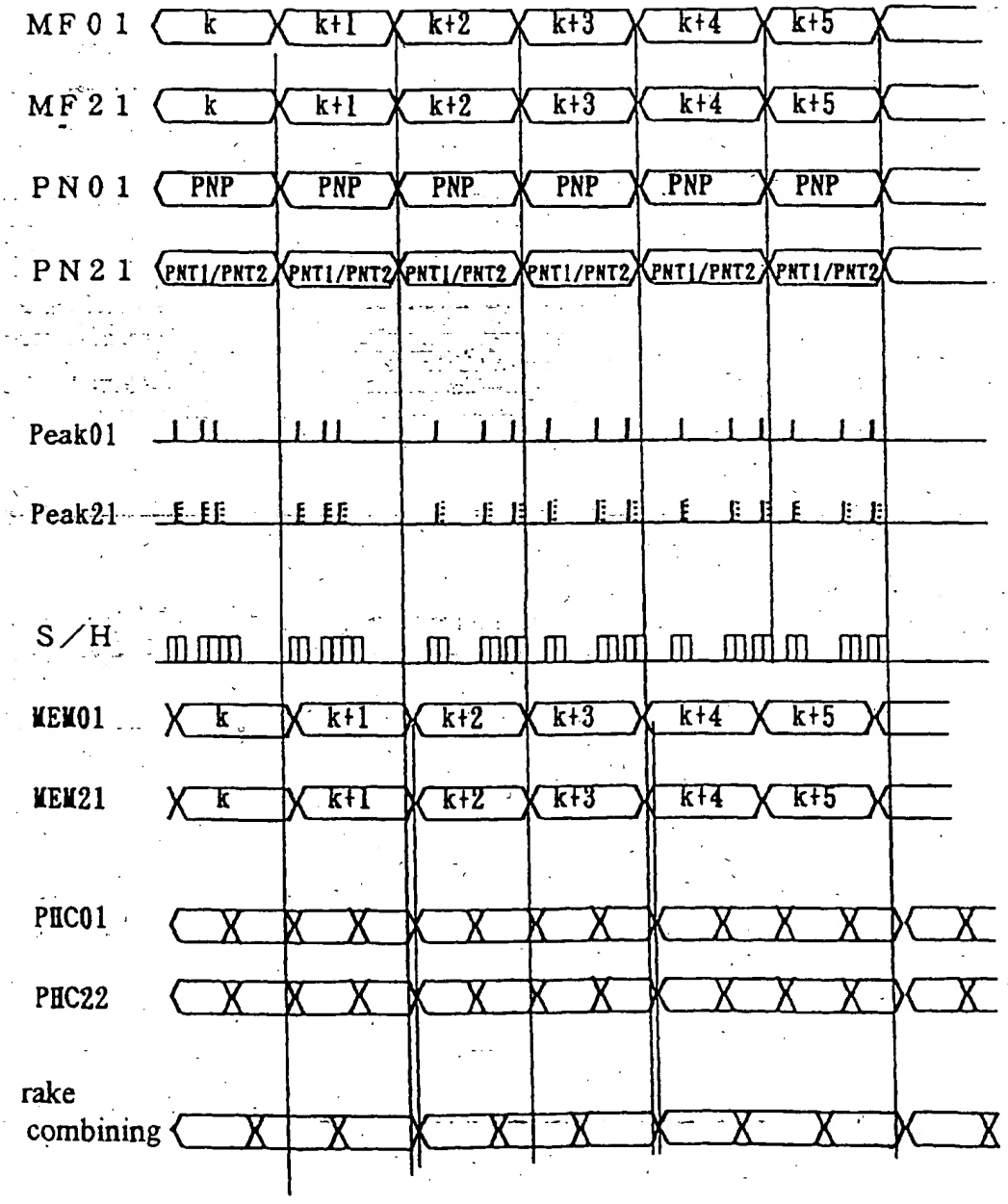

MF01
MF21
PN01
PN21
Peak01
Peak21
S/H
MEM01
MEM21
PHC01
PHC22
rake combining
k
k+1
k+2
k+3
k+4
k+5
PNP
PNT1/PNT2

Fig. 11

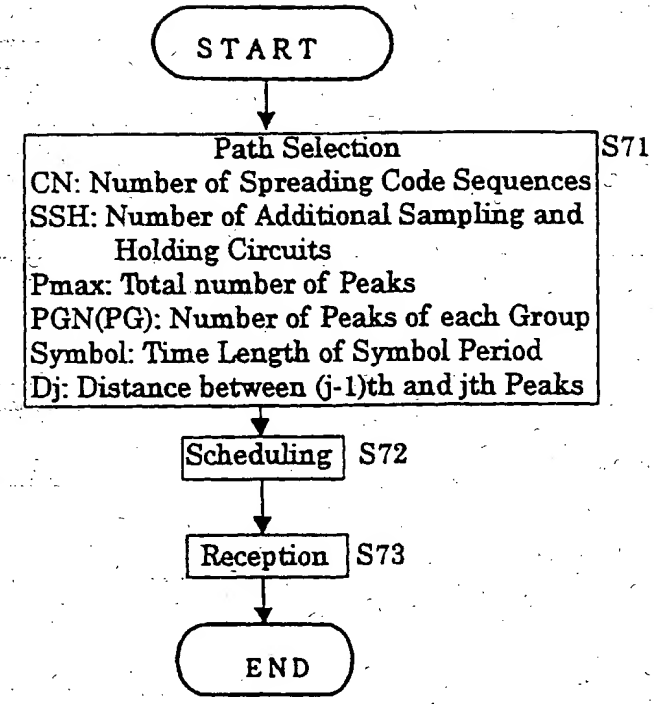

START
Path Selection
CN: Number of Spreading Code Sequences
SSH: Number of Additional Sampling and Holding Circuits
Pmax: Total number of Peaks
PGN(PG): Number of Peaks of each Group
Symbol: Time Length of Symbol Period
Dj: Distance between (j-1)th and jth Peaks
S71
Scheduling
S72
Reception
S73
END

Fig.12

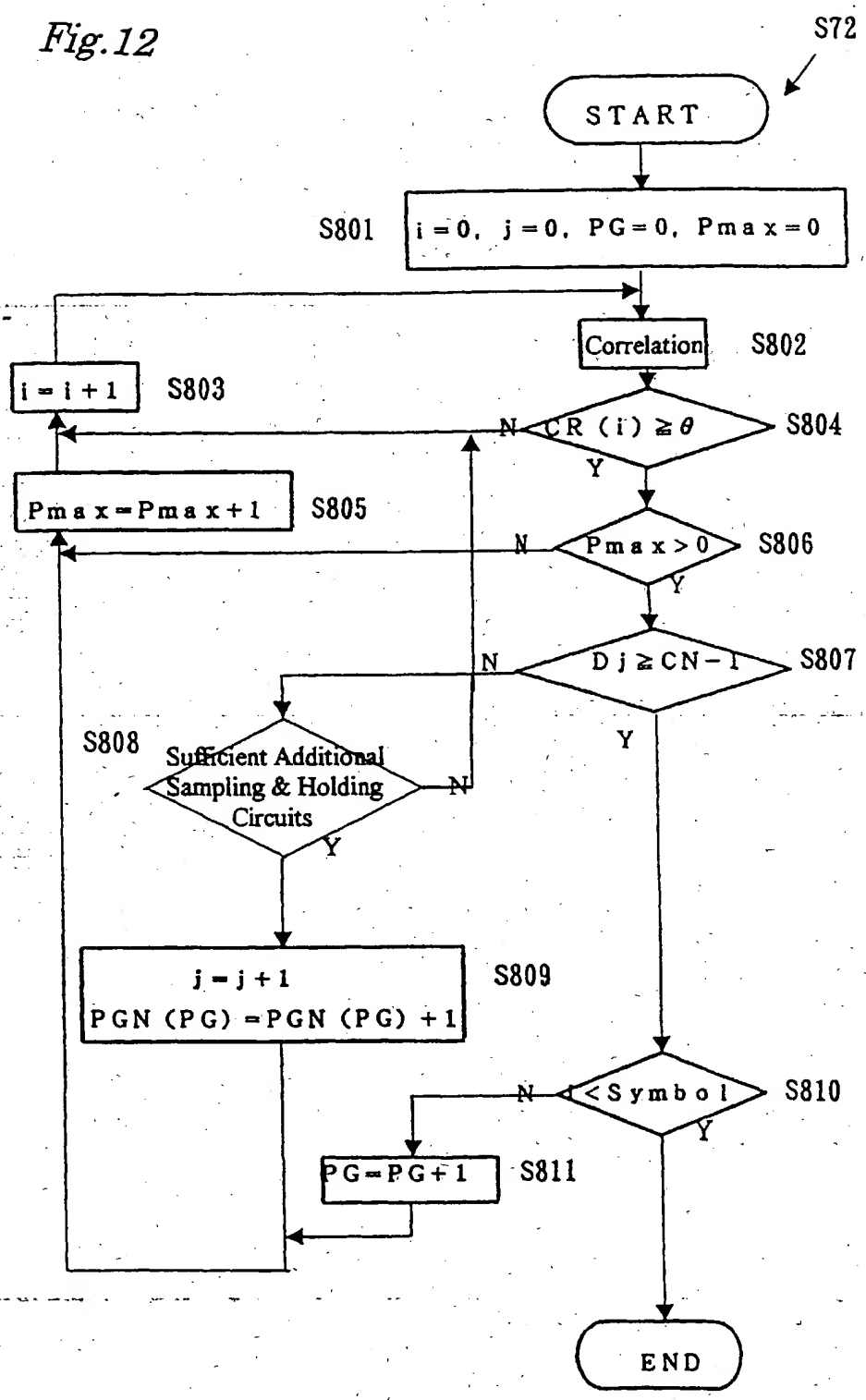

S72
START
S801
i = 0, j = 0, PG = 0, Pmax = 0
Correlation
S802
i = i + 1
S803
N
CR (i) ≧ θ
S804
Y
Pmax = Pmax + 1
S805
N
Pmax > 0
S806
Y
N
Dj ≧ CN − 1
S807
Y
S808
Sufficient Additional Sampling & Holding Circuits
N
Y
j = j + 1
PGN (PG) = PGN (PG) + 1
S809
N
< Symbol
S810
Y
PG = PG + 1
S811
END

Fig.13

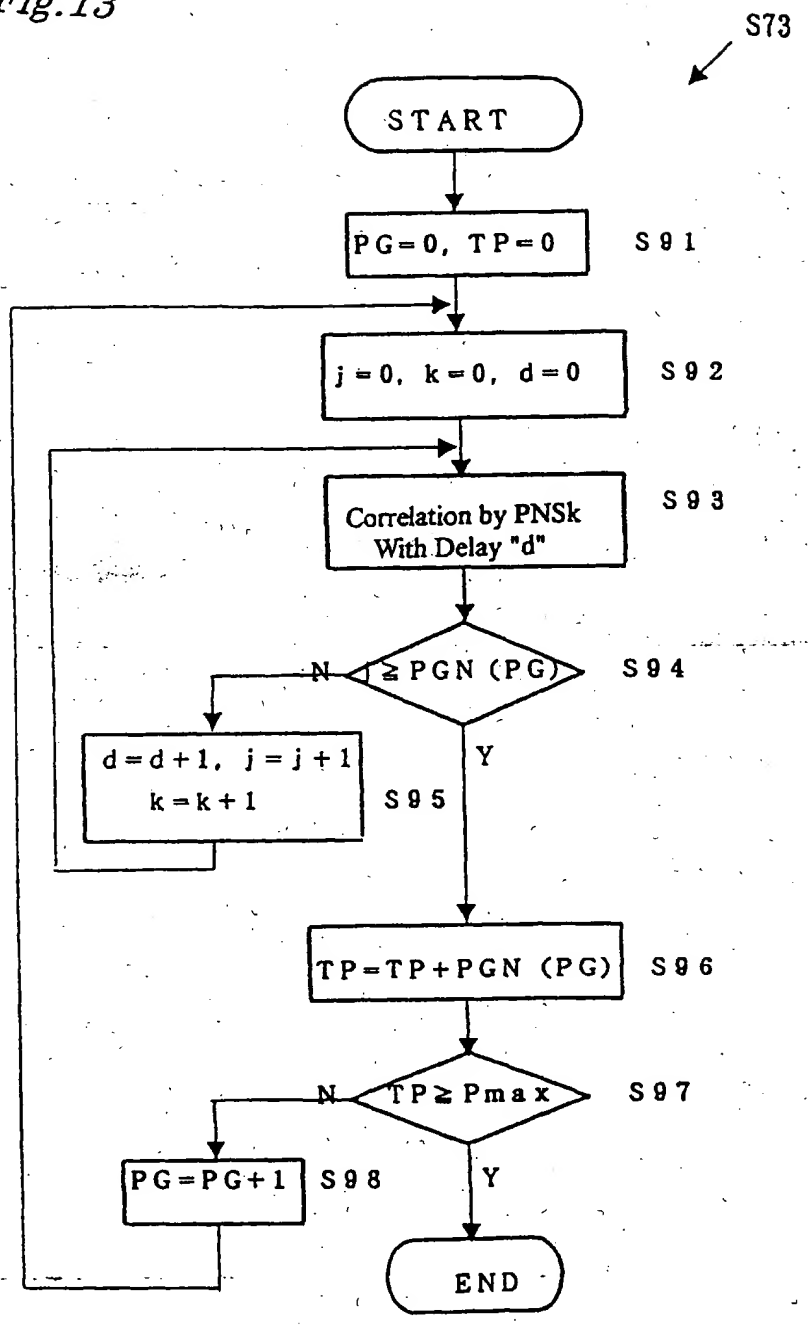

S73
START
PG=0, TP=0
S91
j=0, k=0, d=0
S92
Correlation by PNSk
With Delay "d"
S93
N
≧PGN (PG)
S94
Y
d=d+1, j=j+1
k=k+1
S95
TP=TP+PGN (PG)
S96
N
TP≧Pmax
S97
Y
PG=PG+1
S98
END

Fig.14

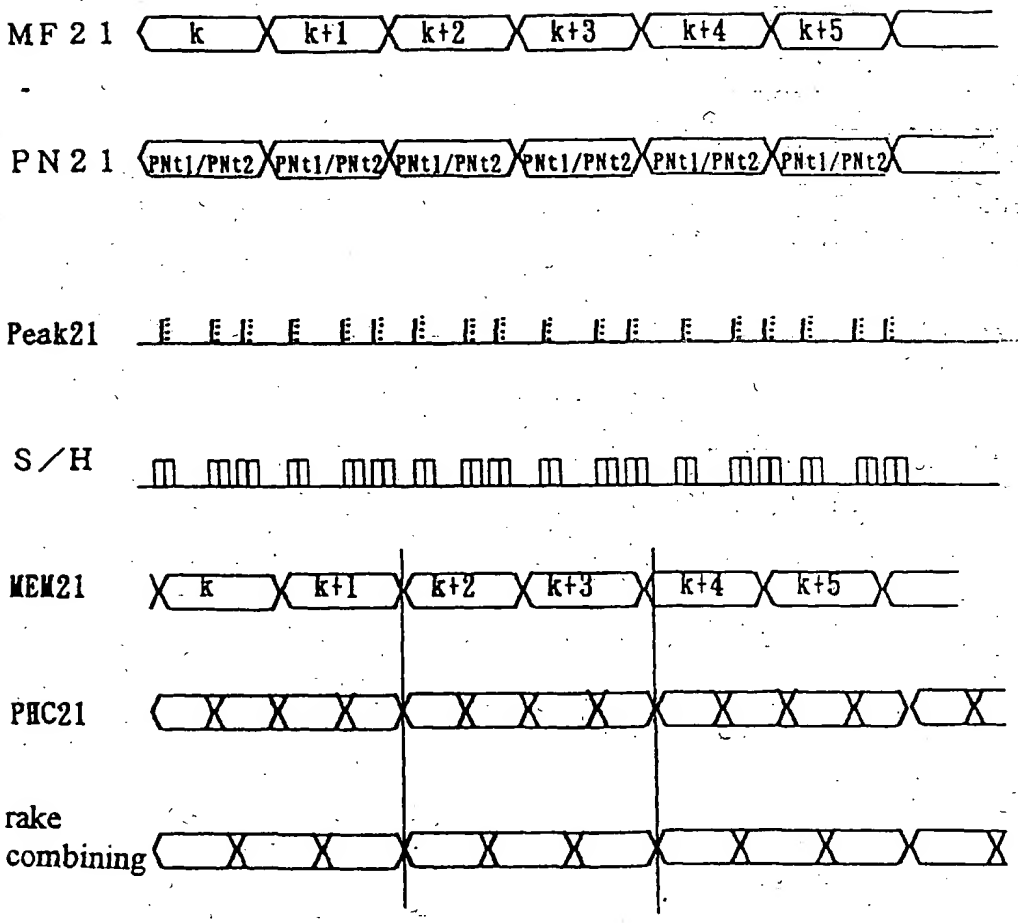

MF21
k
k+1
k+2
k+3
k+4
k+5
PN21
PNt1/PNt2
Peak21
S/H
MEM21
PHC21
rake
combining

Fig.15

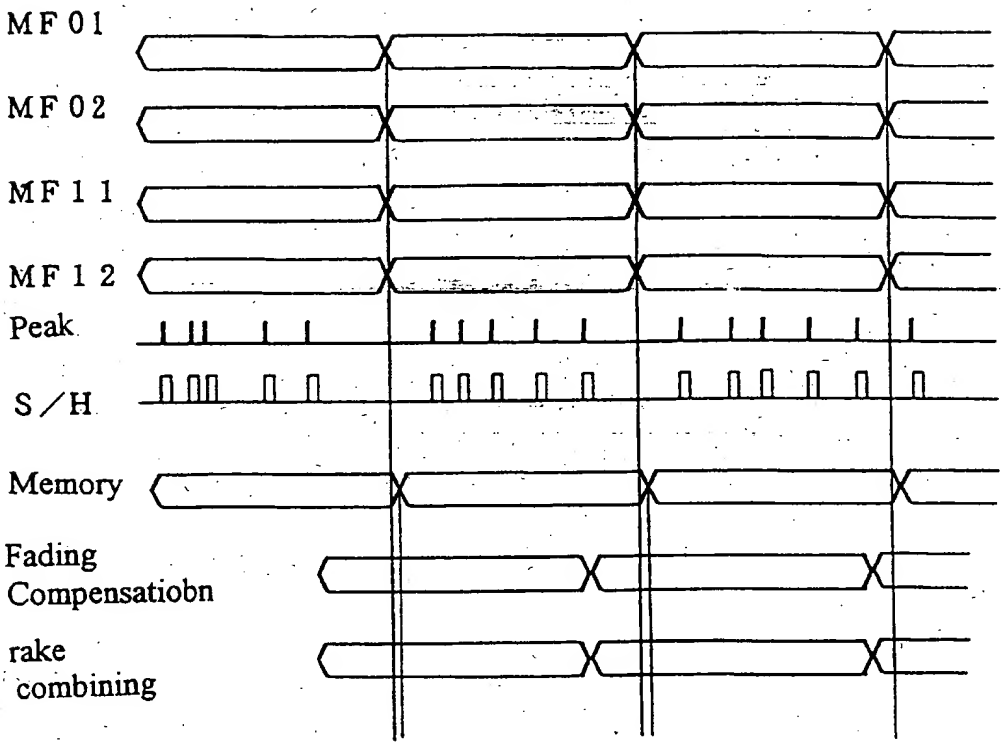

MF01
MF02
MF11
MF12
Peak
S/H
Memory
Fading
Compensatiobn
rake
combining

Fig.16

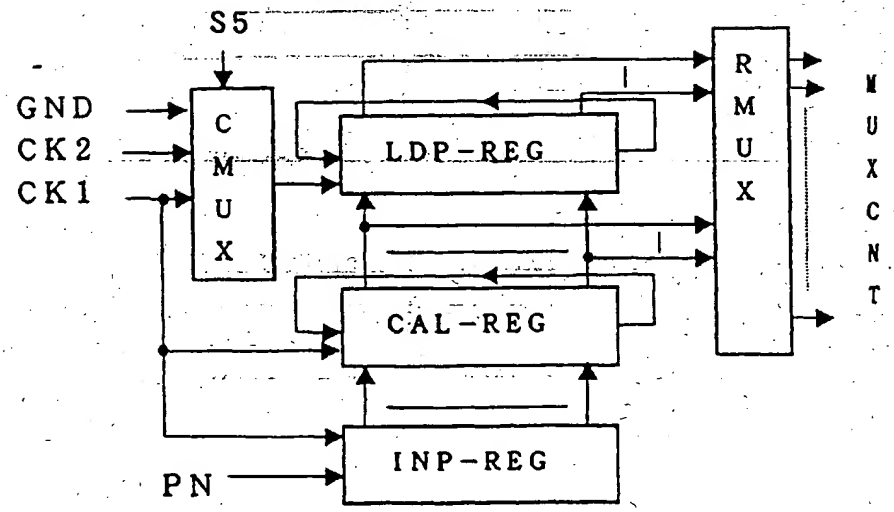


Fig.17

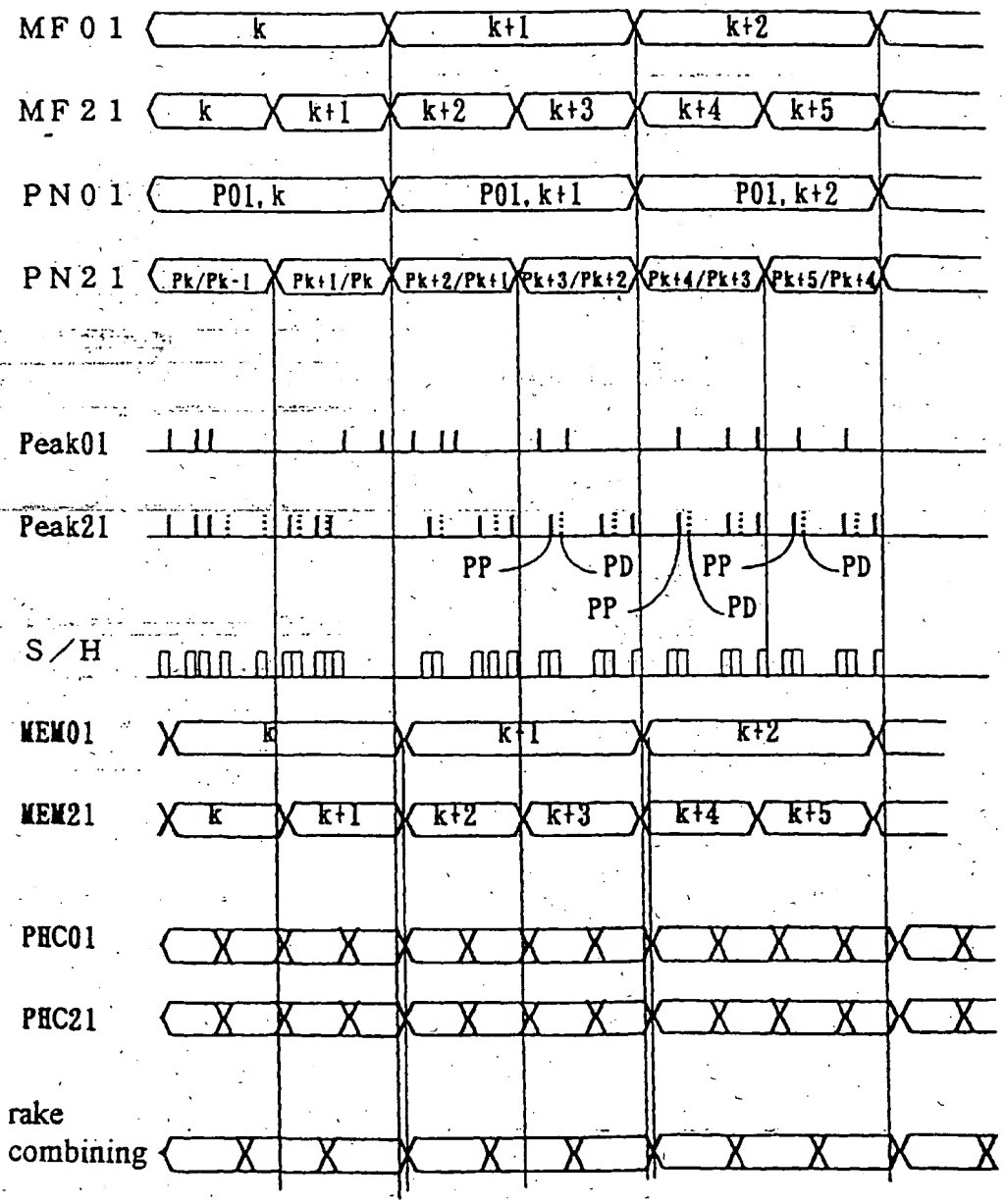

MF01
k
k+1
k+2
MF21
k
k+1
k+2
k+3
k+4
k+5
PN01
P01, k
P01, k+1
P01, k+2
PN21
Pk/Pk-1
Pk+1/Pk
Pk+2/Pk+1
Pk+3/Pk+2
Pk+4/Pk+3
Pk+5/Pk+4
Peak01
Peak21
PP
PD
PP
PD
PP
PD
S/H
MEM01
k
k+1
k+2
MEM21
k
k+1
k+2
k+3
k+4
k+5
PHC01
PHC21
rake
combining

Fig.18

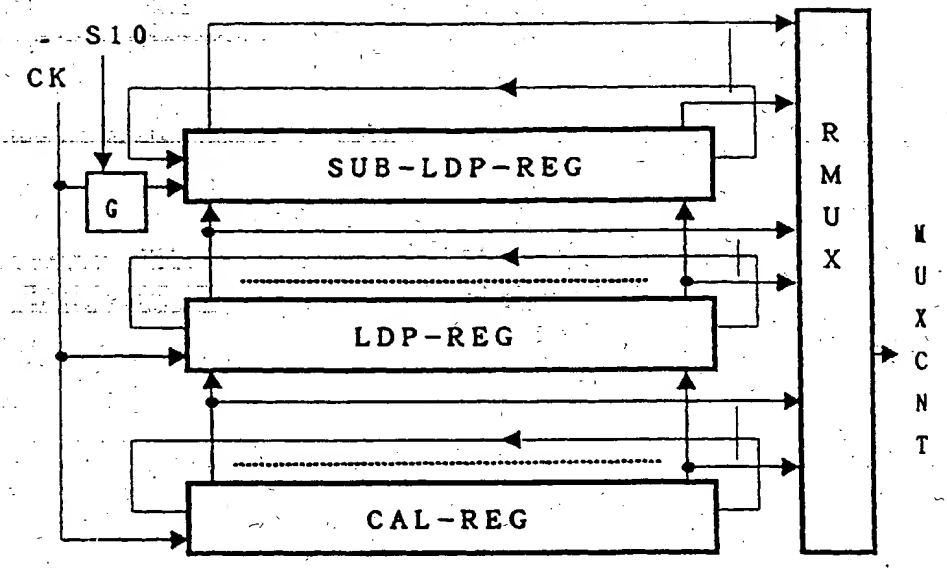


Fig.19

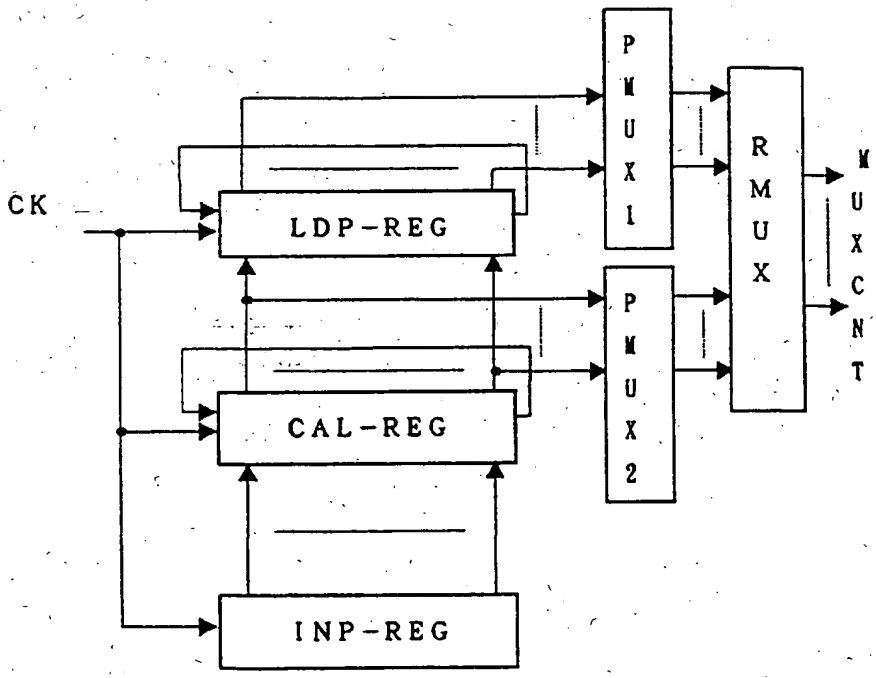


Fig.20

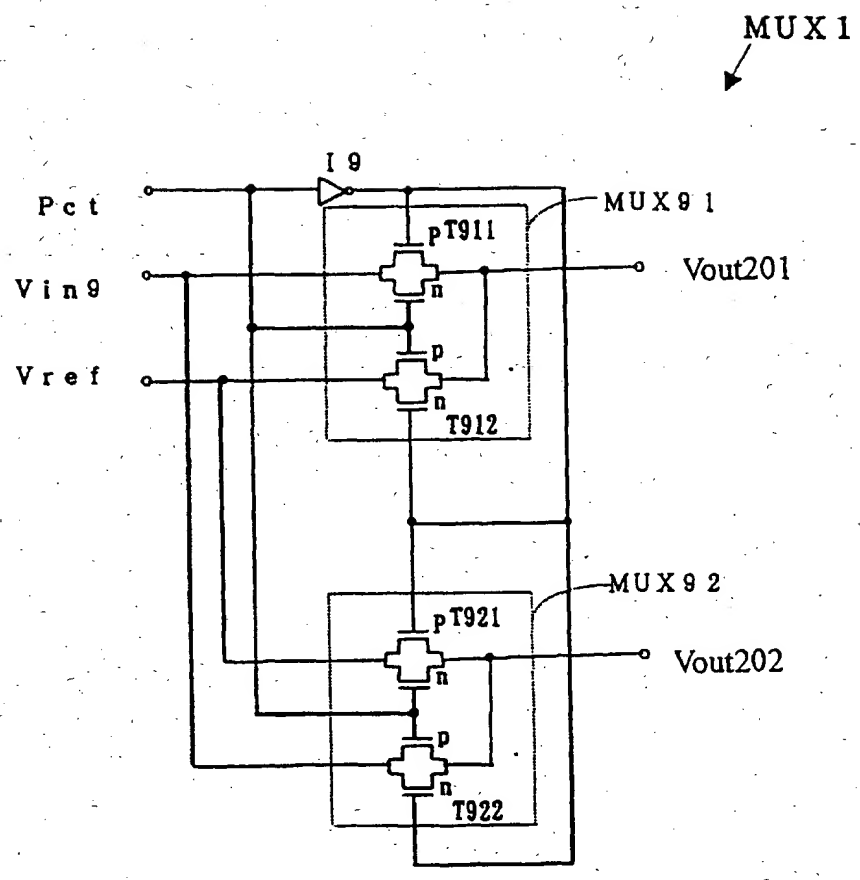

MUX1
I9
Pct
Vin9
Vref
MUX91
pT911
n
Vout201
p
n
T912
MUX92
pT921
n
Vout202
p
n
T922

Fig.21

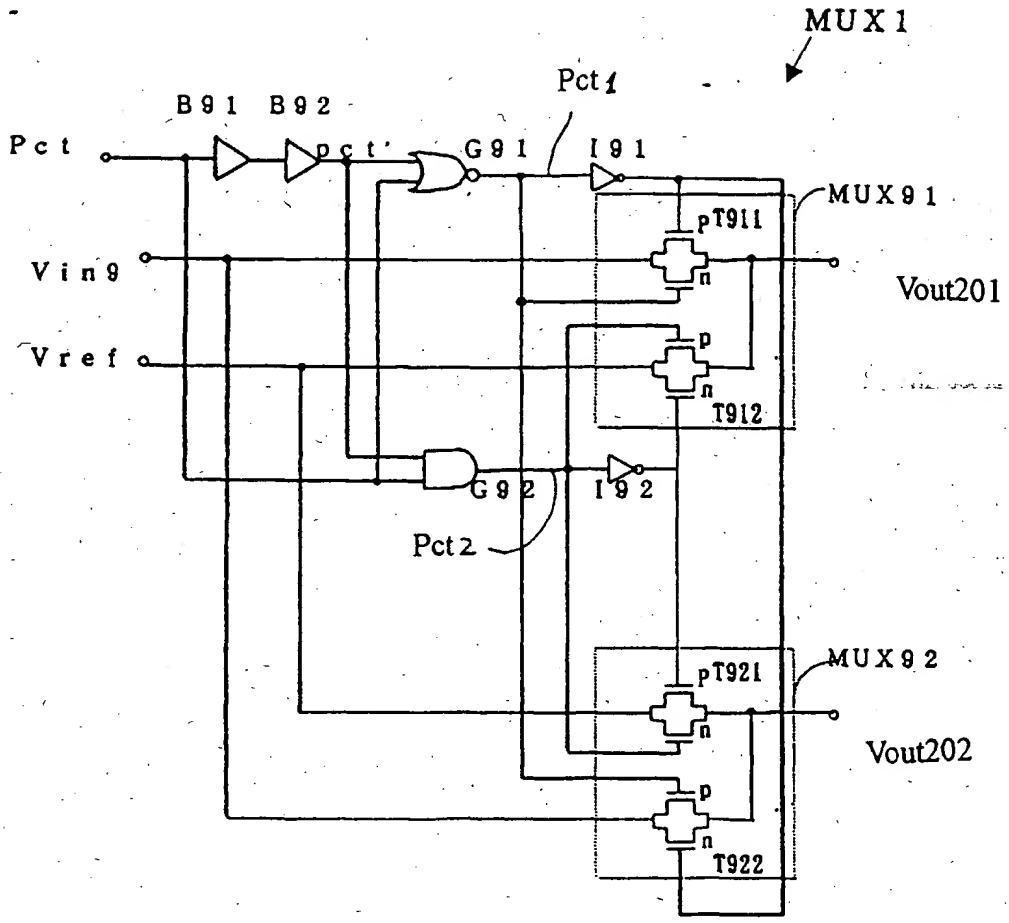

MUX1
Pct1
B91
B92
Pct
pct'
G91
I91
MUX91
pT911
Vin9
Vout201
Vref
T912
G92
I92
Pct2
MUX92
pT921
Vout202
T922

Fig.22

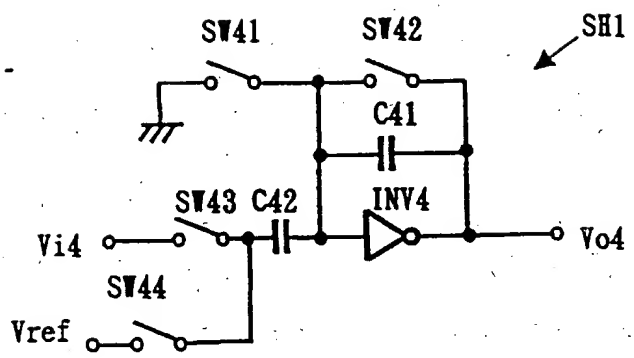

SW41
SW42
SH1
C41
SW43
C42
INV4
Vi4
Vo4
SW44
Vref

Fig.23

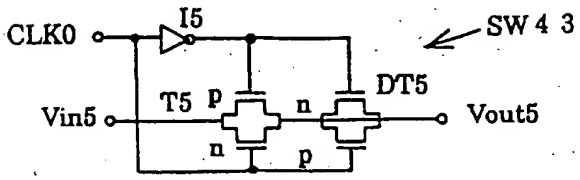
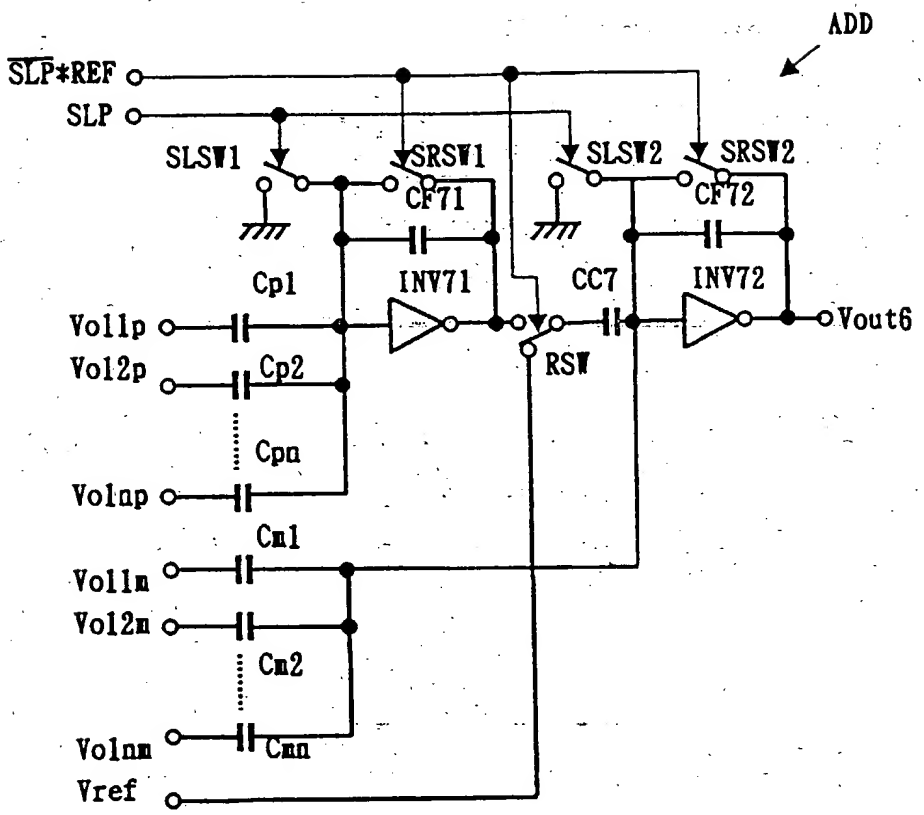

CLK0
I5
SW 4 3
T5
p
DT5
Vin5
n
Vout5
n
p

Fig.24


ADD
SLP*REF
SLP
SLSW1
SRSW1
SLSW2
SRSW2
CF71
CF72
Cp1
INV71
CC7
INV72
Vout6
Vol1p
Vol2p
Cp2
Cpn
Volnp
RSW
Cn1
Vol1n
Vol2n
Cn2
Volnn
Cnn
Vref

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/02637

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H04J13/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H04J13/00-13/06, H04B1/707-1/713

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-2001
Kokai Jitsuyo Shinan Koho 1971-2001 Jitsuyo Shinan Toroku Koho 1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
JOIS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,A	JP, 2000-244456, A (Mitsubishi Electric Corporation), 08 September, 2000 (08.09.00), Full text; all drawings (Family: none)	1-14
A	JP, 11-196067, A (NTT Ido Tsushinmo K.K.), 21 July, 1999 (21.07.99), Full text; all drawings & EP, 932262, A2	1-14
A	JP, 11-274977, A (Sharp Corporation), 08 October, 1999 (08.10.99), Full text; all drawings (Family: none)	1-14
A	JP, 10-285079, A (Hitachi, Ltd.), 23 October, 1998 (23.10.98), Full text; all drawings (Family: none)	1-14
A	JP, 10-173485, A (Mitsubishi Electric Corporation), 26 June, 1998 (26.06.98), Full text; all drawings & US, 5903595, A	1-14

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 June, 2001 (22.06.01)	03 July, 2001 (03.07.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)